

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SANTANA - M51 MLB

PRODUCTION RELEASED

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
M		508667	PRODUCTION RELEASED	06/04/07	06/22/04

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17	17	NB Power 2	M51_HENRY	08/04/2006
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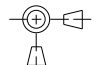
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46	60	LPC+ CONN	M51_HENRY	08/04/2006
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60	77	PWR GOOD	M51_PAUL	08/04/2006
61	78	3V DC/DC 2.5V	M51_PAUL	08/04/2006
62	79	1.8V & 1.2V VREG	M51_PAUL	08/04/2006
63	80	1.5V_S0 & 1.05V_S0 VREG	M51_PAUL	08/04/2006
64	82	5V DC/DC	M51_PAUL	08/04/2006
65	83	S0 AND S3 FETS	M51_PAUL	08/04/2006
66	84	MXM PCI-E & PWR	M51_DAVE (MASTER)	
67	85	MXM I/O	M51_DAVE (MASTER)	
68	94	Internal Display Conns	M51_DAVE (MASTER)	
69	97	External Display Conns	M51_DAVE (MASTER)	

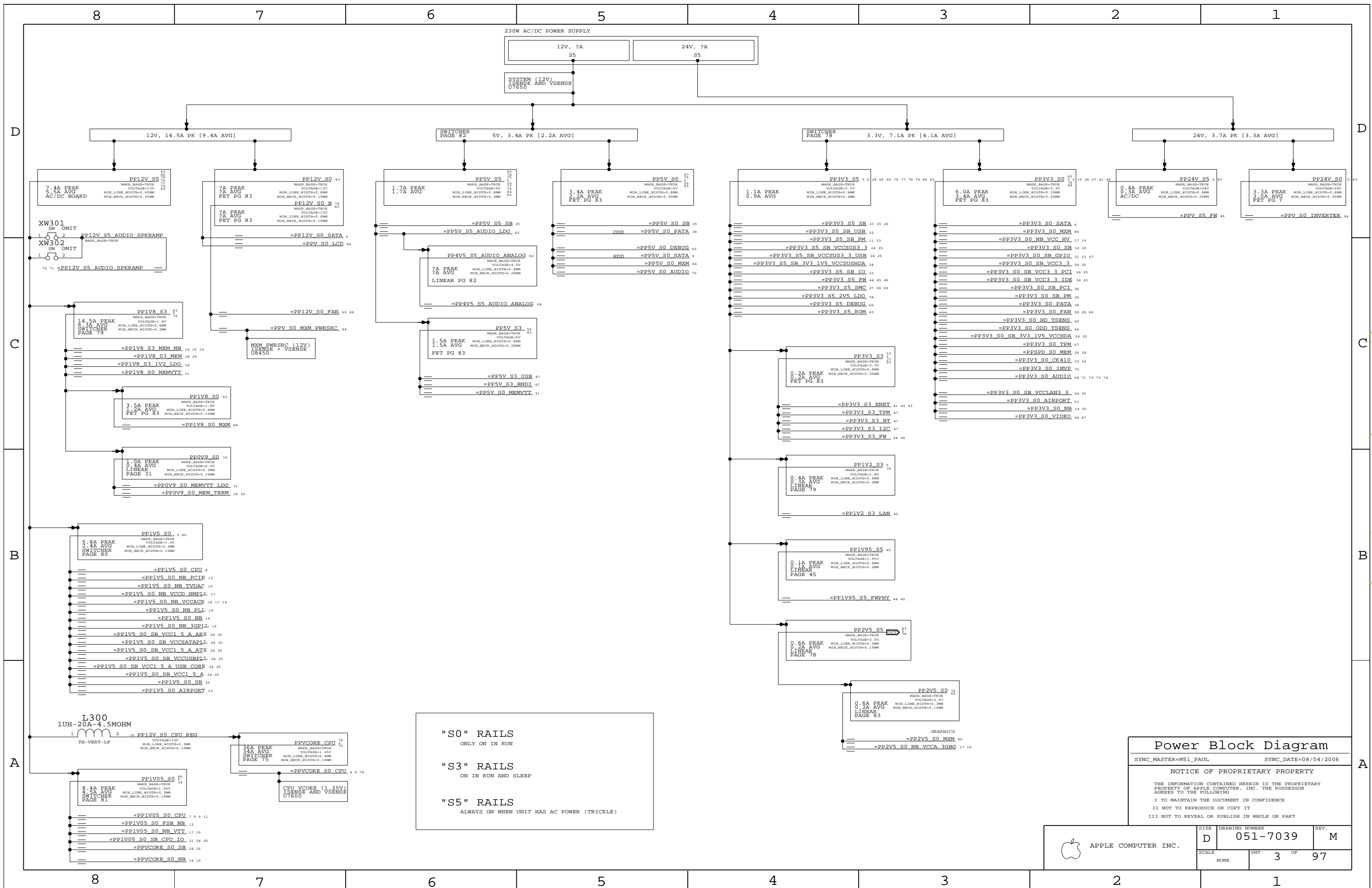
Schematic / PCB #'s

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-7039	1	PCB, SCHEM, MLB, M51	SCH1		
820-1984	1	PCB, FAB, MLB, M51	MLB1		

NEW M51 630 BOMS 9/7
CURRENT: REV F 11/13
SCH: REV K

M51A REV A 11/13
M51A CANCELLED 1/16/07
NEW BOOTROM & BOMS 1/16/07

DIMENSIONS ARE IN MILLIMETERS		METRIC		Apple Computer Inc.	
XX : _____		DRAPTER	DESIGN CK	NOTICE OF PROPRIETARY PROPERTY THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I. TO MAINTAIN THE DOCUMENT IN CONFIDENCE II. NOT TO REPRODUCE OR COPY IT III. NOT TO REVEAL OR PUBLISH IN WHOLE OR PART	
X.XX : _____		ENG APPD	MFG APPD		
X.XXX : _____		QA APPD	DESIGNER		
ANGLES : _____		RELEASE	SCALE		
DO NOT SCALE DRAWING		NONE		TITLE	
 THIRD ANGLE PROJECTION		MATERIAL/FINISH NOTED AS APPLICABLE		SIZE D	DRAWING NUMBER 051-7039
				REV. M	SHT 1 OF 97



"S0" RAILS
ONLY ON IN RUN

"S3" RAILS
ON IN RUN AND SLEEP

"S5" RAILS
ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)

Power Block Diagram

SYNC_MASTER=M51_PAUL SYNC_DATE=08/04/2006

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7039	M
SCALE	SHT	OF	
NONE	3	97	

Production BOM

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7899	PCBA,MLB,2.33GHZ,M51	M51_COMMON,M51_BEST,EEE_WZD,PRODUCTION,M51
630-7898	PCBA,MLB,2.16GHZ,M51	M51_COMMON,M51_BETTER,EEE_WZC,PRODUCTION,M51
630-8043	PCBA,MLB,2.33GHZ,M51,NEWROM,EEE:XCX	M51_COMMON,M51_BEST,EEE_XCX,PRODUCTION,M51A
630-8673	PCBA,MLB,2.16GHZ,M51,NEWROM,EEE:XY9	M51_COMMON,M51_BETTER,EEE_XY9,PRODUCTION,M51A

TOP TWO BOMS WERE INITIAL M51 PRODUCTION

BOTTOM TWO USED TO BE M51A, THEN M51 WAS CANCELLED SO THESE JUST TRACK A NEW BOOT ROM

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0086	126S0078		ALL	Sanyo alt for Nich.
126S0099	126S0073		ALL	Sanyo alt for Nich.
126S0068	126S0088		ALL	Sanyo alt for Nich.
124-0361	124-0339		ALL	SANYO ALT

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
378S0141	378S0140		ALL	GREEN LED ALT.
353S1461	353S1465		U7500	CPU VREG NEW REV
740S0044	740S0028		F9710	DVI DDC (LITTLEFUSE)
138S0567	138S0516		ALL	CAP CONSOLIDATION
376S0388	376S0444		ALL	ON SEMI 2ND SRC FOR IR
138S0608	138S0576		ALL	2ND SRC FOR SUPPLY

Development BOM

BOM NUMBER	BOM NAME	BOM OPTIONS
603-8960	PCBA,DEVBOM,M51	M51_DEVELOPMENT

BOMOPTION Groups

BOM GROUP	BOM OPTIONS
M51_COMMON	COMMON,M51_COMMON1,M51_COMMON2,ALTERNATE
M51_COMMON1	CPU_TSSENS_EXT,GPU_TSSENS_INT,GPU_TSSENS_EXT,MXM_ROM,NBCFG_PEG_REVERSE
M51_COMMON2	SB_SYSRST_4_PVT,ITP,MEROM,AMB_TSSENS,CPU_PWR_SENSE
M51_DEVELOPMENT	DEVELOPMENT,M51_DEV1
M51_DEV1	CPU_TSSENS_INT,SYS_PWR_SENSE,MXM_PWR_SENSE

BarCode Label / EEE #'s

MEROM BOM OPTION DUE TO PAGE 76 SHARING W/ M50

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-6447	1	BAR CODE LABEL, MLB, M51	[EEE:WZD]	CRITICAL	EEE_WZD
825-6447	1	BAR CODE LABEL, MLB, M51	[EEE:WZC]	CRITICAL	EEE_WZC
825-6447	1	BAR CODE LABEL, MLB, M51	[EEE:XCX]	CRITICAL	EEE_XCX
825-6447	1	BAR CODE LABEL, MLB, M51	[EEE:XY9]	CRITICAL	EEE_XY9

SENSOR STUFFING OPTIONS

MUST STUFF WHEN SYS_PWR_SENSE IS NOT STUFFED (I.E. WHEN DEVELOPMENT BOM IS NOT STUFFED)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
102S0699	1	RES,0-OHM,2010	R7650	PRODUCTION
116S0090	1	RES,10K-OHM,5%,0402	C7650	PRODUCTION
116S0090	1	RES,10K-OHM,5%,0402	C7650	PRODUCTION

PULL-DOWNS FOR UNUSED PINS WHEN DEVELOPMENT SENSORS ARE GONE

MUST STUFF WHEN MXM_PWR_SENSE IS NOT STUFFED (IF THIS MOVES TO DEV BOM)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
107S0070	1	RES,0-OHM,2512	R8450	PRODUCTION
116S0090	1	RES,10K-OHM,5%,0402	C8458	PRODUCTION
116S0090	1	RES,10K-OHM,5%,0402	C8459	PRODUCTION

PULL-DOWNS FOR UNUSED PINS WHEN DEVELOPMENT SENSORS ARE GONE

MUST STUFF WHEN CPU_PWR_SENSE IS NOT STUFFED (IF THIS MOVES TO DEV BOM)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S0090	1	RES,10K-OHM,5%,0402	C7602	NOSTUFF
116S0090	1	RES,10K-OHM,5%,0402	C7612	NOSTUFF

PULL-DOWNS FOR UNUSED PINS WHEN DEVELOPMENT SENSORS ARE GONE

CHIPSET, ROMS, ETC.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
511S0025	1	IC,CPU-SKT,479BGA	J0700	CRITICAL	
338S0328	1	IC,945PM,NORTHBRIDGE	U1200	CRITICAL	
343S0385	1	IC,SB,652BGA	U2100	CRITICAL	
359S0117	1	IC,SLG84435,CLK GEN,68PIN QFN	U3301	CRITICAL	
338S0270	1	IC,88E8053,GIGABIT ENET XCVR,64P QFN,NO	U4101	CRITICAL	
(335S0382) 341S1797	1	IC,ENET LAN ROM	U4102	CRITICAL	
341S1789	1	IC,TPM,TSSOP,28P	U6700	CRITICAL	TPM
353S1465	1	IC,CPU VREG,IMVP,TWO PHASE,SCREENED	U7500	CRITICAL	
341S1892	1	IC,2K I2C EEPROM,MXM,M51	U8570	CRITICAL	MXM_ROM
(335S0384) 341T0019	1	IC,EFI BOOT ROM,M51	U6301	CRITICAL	M51
341T0060	1	IC,EFI BOOT ROM,M51A	U6301	CRITICAL	M51A
(338S0274) 341T0020	1	IC,SMC,M51	U5800	CRITICAL	

PROCESSORS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3392	1	MEROM 2.33GHZ, M51	CPU	CRITICAL	M51_BEST
337S3390	1	MEROM 2.16GHZ, M51	CPU	CRITICAL	M51_BETTER

Misc. Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
742-0048	1	BAT,COIN,3V,220MAH,CR2032	BT2600	CRITICAL	NOSTUFF
820-2038	1	IO ALIGNMENT BOARD, M51	PCB2	CRITICAL	
946-0743	1	IO ALIGNMENT BOARD ADHESIVE	ADH1	CRITICAL	

BATTERY IS INSTALLED AT FATP

BOM Config

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

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	D	051-7039	M
SCALE	SHT	OF	
NONE	4	97	

8

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2

1

LAYOUT: PLACE CLOSE TO DESTINATION
* OPPOSITE END FROM CLOCK BUFFER

FSB SIGNALS

34 21 SB_CLK100M_SATA_P PP6C4 OMIT P4MM
34 21 SB_CLK100M_SATA_N PP6C5 OMIT P4MM

12 11 7 FSB_CPURST_L PP621 OMIT P4MM

1473 NC_NB_CFG<17> MAKE_BASE=TRUE
1474 NC_NB_CFG<15> MAKE_BASE=TRUE
1475 NC_NB_CFG<14> MAKE_BASE=TRUE
1476 NC_NB_CFG<13> MAKE_BASE=TRUE
1477 NC_NB_CFG<12> MAKE_BASE=TRUE
1478 NC_NB_CFG<11> MAKE_BASE=TRUE
1479 NC_NB_CFG<10> MAKE_BASE=TRUE
1480 NC_NB_CFG<8> MAKE_BASE=TRUE
1481 NC_NB_CFG<6> MAKE_BASE=TRUE
1482 NC_NB_CFG<4> MAKE_BASE=TRUE
1483 NC_NB_CFG<3> MAKE_BASE=TRUE

PPVCORE_CPU FUNC_TEST=TRUE
PP3V3_S5 FUNC_TEST=TRUE
PP2V5_S5 FUNC_TEST=TRUE
PP1V8_S3 FUNC_TEST=TRUE
PP1V2_S3 FUNC_TEST=TRUE
PP1V5_S0 FUNC_TEST=TRUE
PP1V05_S0 FUNC_TEST=TRUE
PP5V_S5 FUNC_TEST=TRUE
PP5V_S0 FUNC_TEST=TRUE
PP3V3_S5 FUNC_TEST=TRUE
PP3V3_S0 FUNC_TEST=TRUE
PP24V_S0 FUNC_TEST=TRUE

XDP_BPM_L<3> FUNC_TEST=TRUE
XDP_BPM_L<2> FUNC_TEST=TRUE
XDP_BPM_L<1> FUNC_TEST=TRUE
XDP_BPM_L<0> FUNC_TEST=TRUE
XDP_DRRSST_L FUNC_TEST=TRUE
SW_RST_BTN_L FUNC_TEST=TRUE
POWER_BUTTON_L FUNC_TEST=TRUE
LPC_AD<0> FUNC_TEST=TRUE
LPC_AD<1> FUNC_TEST=TRUE
LPC_AD<2> FUNC_TEST=TRUE
LPC_AD<3> FUNC_TEST=TRUE
LPC_FRAME_L FUNC_TEST=TRUE
PM_CLKRUN_L FUNC_TEST=TRUE
BOOT_LPC_SPI_L FUNC_TEST=TRUE
DEBUG_RST_L FUNC_TEST=TRUE
FWH_INIT_L FUNC_TEST=TRUE
PCI_CLK_PORT80 FUNC_TEST=TRUE
INT_SERIRQ FUNC_TEST=TRUE
PM_SUS_STAT_L FUNC_TEST=TRUE
SMC_MD1 FUNC_TEST=TRUE
SMC_RST_L FUNC_TEST=TRUE
SMC_NMI FUNC_TEST=TRUE
SV_SET_UP FUNC_TEST=TRUE
ISENSE_CAL_EN FUNC_TEST=TRUE
INV_ENABLE_BL FUNC_TEST=TRUE
LCD_PWM FUNC_TEST=TRUE
CPU_VID<0> FUNC_TEST=TRUE
CPU_VID<1> FUNC_TEST=TRUE
CPU_VID<2> FUNC_TEST=TRUE
CPU_VID<3> FUNC_TEST=TRUE
CPU_VID<4> FUNC_TEST=TRUE
CPU_VID<5> FUNC_TEST=TRUE
CPU_VID<6> FUNC_TEST=TRUE
PM_DPRSIPVR FUNC_TEST=TRUE
CPU_DPRSTP_L FUNC_TEST=TRUE
VR_PWRGOOD_DELAY FUNC_TEST=TRUE
VR_PWRGD_CK410 FUNC_TEST=TRUE
ALL_SYS_PWRGD FUNC_TEST=TRUE
PM_SLP_S4_L FUNC_TEST=TRUE
PM_SLP_S3_L FUNC_TEST=TRUE

SMC_TCK FUNC_TEST=TRUE
SMC_TDI FUNC_TEST=TRUE
SMC_TDO FUNC_TEST=TRUE
SMC_TMS FUNC_TEST=TRUE
SMC_TRST_L FUNC_TEST=TRUE
SMC_TX_L FUNC_TEST=TRUE
SMC_RX_L FUNC_TEST=TRUE
SMC_MANUAL_RST_L FUNC_TEST=TRUE
XDP_TCK FUNC_TEST=TRUE
XDP_TDI FUNC_TEST=TRUE
XDP_TDO FUNC_TEST=TRUE
XDP_TMS FUNC_TEST=TRUE
XDP_TRST_L FUNC_TEST=TRUE
POWER_BUTTON_L FUNC_TEST=TRUE
SW_RST_BTN_L FUNC_TEST=TRUE
NB_TSENS_HS_DXP FUNC_TEST=TRUE
NB_TSENS_HS_DYN FUNC_TEST=TRUE
CPU_XDP_CLK_N FUNC_TEST=TRUE
CPU_XDP_CLK_P FUNC_TEST=TRUE
ITPRESET_L FUNC_TEST=TRUE
XDP_BPM_L<5> FUNC_TEST=TRUE
XDP_BPM_L<4> FUNC_TEST=TRUE

I513 TP_PCI_GNT3_L MAKE_BASE=TRUE
PCI_GNT3_L

SPARE_USB_PORT
USB_F_N TP_USB_F_N MAKE_BASE=TRUE
USB_F_P TP_USB_F_P MAKE_BASE=TRUE

I513 TP_LVDS_BKLTEN MAKE_BASE=TRUE
LVDS_BKLTEN

NC_AUD_BI_PORT_G_L NO_TEST=TRUE
NC_ALS_GAIN NO_TEST=TRUE
NC_AUD_VREF_PORT_C NO_TEST=TRUE
NC_AUD_VREF_PORT_D NO_TEST=TRUE
NC_SMC_BATT_CHG_EN NO_TEST=TRUE
NC_SMC_BATT_ISET NO_TEST=TRUE
NC_SMC_BATT_TRICKLE_EN_L NO_TEST=TRUE
NC_SMC_BATT_VSET NO_TEST=TRUE
NC_SMC_P20 NO_TEST=TRUE
NC_SMC_P21 NO_TEST=TRUE
NC_SMC_P22 NO_TEST=TRUE
NC_SMC_P23 NO_TEST=TRUE
NC_SMC_P26 NO_TEST=TRUE
NC_SMC_P27 NO_TEST=TRUE
NC_SMC_SYS_ISET NO_TEST=TRUE
NC_SMC_SYS_VSET NO_TEST=TRUE
NC_SMS_X_AXIS NO_TEST=TRUE
NC_SMS_Y_AXIS NO_TEST=TRUE
NC_SMS_Z_AXIS NO_TEST=TRUE

NC_J7302_3 NO_TEST=TRUE
NC_J7302_6 NO_TEST=TRUE
NC_AUD_BI_PORT_E_L NO_TEST=TRUE
NC_AUD_BI_PORT_E_R NO_TEST=TRUE
NC_SMC_MEM_ISENSE NO_TEST=TRUE
NC_AUD_BI_PORT_H_L NO_TEST=TRUE
NC_AUD_BI_PORT_H_R NO_TEST=TRUE
NC_AUD_VREF_PORT_B NO_TEST=TRUE

TP_MEM_B_A<15> NO_TEST=TRUE
TP_MEM_B_A<14> NO_TEST=TRUE

PEG_R2D_C_N<0> NO_TEST=TRUE
PEG_R2D_C_P<0> NO_TEST=TRUE
PEG_R2D_C_N<1> NO_TEST=TRUE
PEG_R2D_C_P<1> NO_TEST=TRUE
PEG_R2D_C_N<2> NO_TEST=TRUE
PEG_R2D_C_P<2> NO_TEST=TRUE
PEG_R2D_C_N<3> NO_TEST=TRUE
PEG_R2D_C_P<3> NO_TEST=TRUE
PEG_R2D_C_N<4> NO_TEST=TRUE
PEG_R2D_C_P<4> NO_TEST=TRUE
PEG_R2D_C_N<5> NO_TEST=TRUE
PEG_R2D_C_P<5> NO_TEST=TRUE
PEG_R2D_C_N<6> NO_TEST=TRUE
PEG_R2D_C_P<6> NO_TEST=TRUE
PEG_R2D_C_N<7> NO_TEST=TRUE
PEG_R2D_C_P<7> NO_TEST=TRUE
PEG_R2D_C_N<8> NO_TEST=TRUE
PEG_R2D_C_P<8> NO_TEST=TRUE
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PEG_R2D_C_P<11> NO_TEST=TRUE
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PEG_R2D_C_P<12> NO_TEST=TRUE
PEG_R2D_C_N<13> NO_TEST=TRUE
PEG_R2D_C_P<13> NO_TEST=TRUE
PEG_R2D_C_N<14> NO_TEST=TRUE
PEG_R2D_C_P<14> NO_TEST=TRUE
PEG_R2D_C_N<15> NO_TEST=TRUE
PEG_R2D_C_P<15> NO_TEST=TRUE

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PEG_R2D_P<0> NO_TEST=TRUE
PEG_R2D_N<1> NO_TEST=TRUE
PEG_R2D_P<1> NO_TEST=TRUE
PEG_R2D_N<2> NO_TEST=TRUE
PEG_R2D_P<2> NO_TEST=TRUE
PEG_R2D_N<3> NO_TEST=TRUE
PEG_R2D_P<3> NO_TEST=TRUE
PEG_R2D_N<4> NO_TEST=TRUE
PEG_R2D_P<4> NO_TEST=TRUE
PEG_R2D_N<5> NO_TEST=TRUE
PEG_R2D_P<5> NO_TEST=TRUE
PEG_R2D_N<6> NO_TEST=TRUE
PEG_R2D_P<6> NO_TEST=TRUE
PEG_R2D_N<7> NO_TEST=TRUE
PEG_R2D_P<7> NO_TEST=TRUE
PEG_R2D_N<8> NO_TEST=TRUE
PEG_R2D_P<8> NO_TEST=TRUE
PEG_R2D_N<9> NO_TEST=TRUE
PEG_R2D_P<9> NO_TEST=TRUE
PEG_R2D_N<10> NO_TEST=TRUE
PEG_R2D_P<10> NO_TEST=TRUE
PEG_R2D_N<11> NO_TEST=TRUE
PEG_R2D_P<11> NO_TEST=TRUE
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PEG_R2D_N<13> NO_TEST=TRUE
PEG_R2D_P<13> NO_TEST=TRUE
PEG_R2D_N<14> NO_TEST=TRUE
PEG_R2D_P<14> NO_TEST=TRUE
PEG_R2D_N<15> NO_TEST=TRUE
PEG_R2D_P<15> NO_TEST=TRUE

PEG_D2R_N<0> NO_TEST=TRUE
PEG_D2R_P<0> NO_TEST=TRUE
PEG_D2R_N<1> NO_TEST=TRUE
PEG_D2R_P<1> NO_TEST=TRUE
PEG_D2R_N<2> NO_TEST=TRUE
PEG_D2R_P<2> NO_TEST=TRUE
PEG_D2R_N<3> NO_TEST=TRUE
PEG_D2R_P<3> NO_TEST=TRUE
PEG_D2R_N<4> NO_TEST=TRUE
PEG_D2R_P<4> NO_TEST=TRUE
PEG_D2R_N<5> NO_TEST=TRUE
PEG_D2R_P<5> NO_TEST=TRUE
PEG_D2R_N<6> NO_TEST=TRUE
PEG_D2R_P<6> NO_TEST=TRUE
PEG_D2R_N<7> NO_TEST=TRUE
PEG_D2R_P<7> NO_TEST=TRUE
PEG_D2R_N<8> NO_TEST=TRUE
PEG_D2R_P<8> NO_TEST=TRUE
PEG_D2R_N<9> NO_TEST=TRUE
PEG_D2R_P<9> NO_TEST=TRUE
PEG_D2R_N<10> NO_TEST=TRUE
PEG_D2R_P<10> NO_TEST=TRUE
PEG_D2R_N<11> NO_TEST=TRUE
PEG_D2R_P<11> NO_TEST=TRUE
PEG_D2R_N<12> NO_TEST=TRUE
PEG_D2R_P<12> NO_TEST=TRUE
PEG_D2R_N<13> NO_TEST=TRUE
PEG_D2R_P<13> NO_TEST=TRUE
PEG_D2R_N<14> NO_TEST=TRUE
PEG_D2R_P<14> NO_TEST=TRUE
PEG_D2R_N<15> NO_TEST=TRUE
PEG_D2R_P<15> NO_TEST=TRUE

PCI_CLK_SB PP6D0 OMIT P4MM
PCI_CLK_FW PP626 OMIT P4MM
PCI_CLK_SMC PP627 OMIT P4MM

LAYOUT NOTE: PLACE NEAR NORTHBRIDGE

LAYOUT NOTE: PLACE NEAR SOUTHBRIDGE

VR_PWRGOOD_DELAY PP665 OMIT P4MM
NB_RST_IN_L_R PP666 OMIT P4MM

IDE_PDIO_R_L PP6C6 OMIT P4MM
IDE_PDIO_RDY PP6C7 OMIT P4MM
IDE_PDD<9> PP6C8 OMIT P4MM

DMI_S2N_N<0> PP673 OMIT P4MM
DMI_S2N_P<0> PP674 OMIT P4MM
MEM_VREF_NB_0 PP6E1 OMIT P4MM
MEM_VREF_NB_1 PP675 OMIT P4MM

PCIE_B_D2R_P PP600 OMIT P4MM
PCIE_B_D2R_N PP601 OMIT P4MM
DMI_N2S_P<0> PP6D3 OMIT P4MM
DMI_N2S_N<0> PP6D4 OMIT P4MM

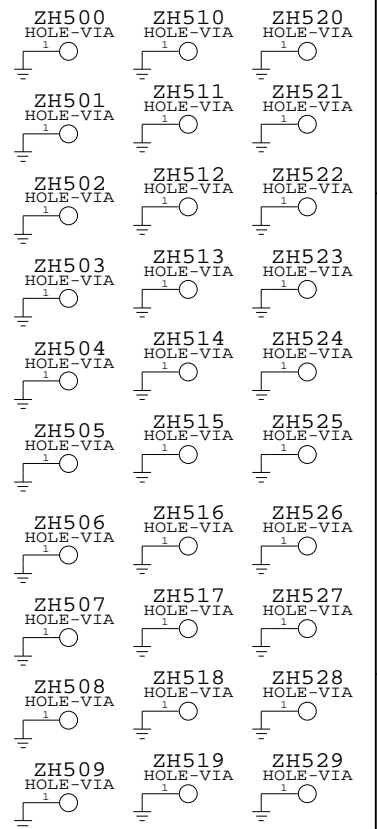
LPC_FRAME_L PP6D8 OMIT P4MM
SPI_S0 PP612 OMIT P4MM
SPI_S1 PP613 OMIT P4MM

ALL I2C BUSES (PLACE IN ACCESSIBLE LOCATION TOP SIDE)

SMBUS_SB_SCL PP604 OMIT P4MM
SMBUS_SB_SDA PP605 OMIT P4MM

SMBUS_SMC_A_S3_SCL PP610 OMIT P4MM
SMBUS_SMC_A_S3_SDA PP611 OMIT P4MM

MISC GROUND VIAS



FUNC TEST 1 OF 2

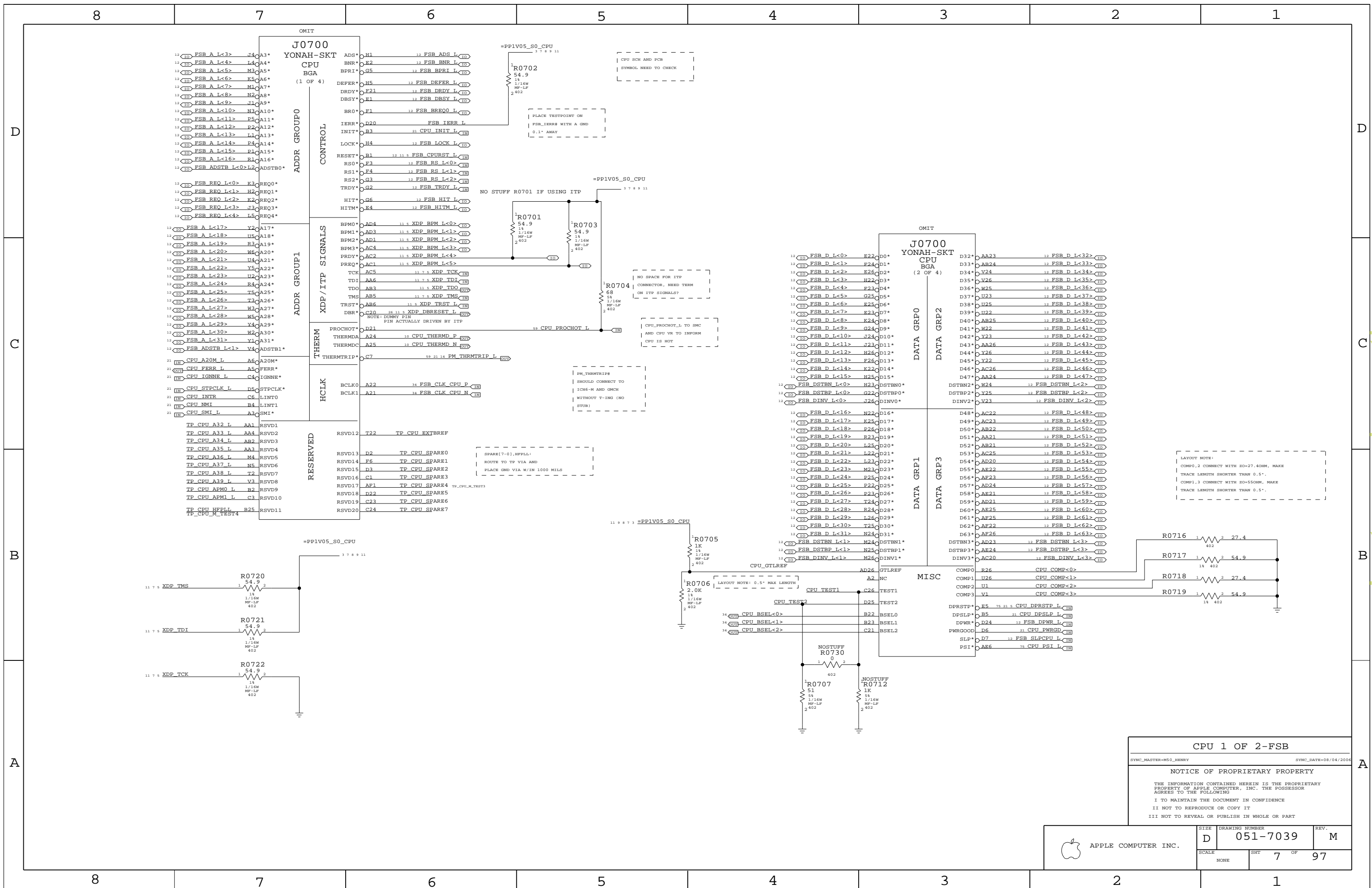
SYNC_MASTER=M51_HENRY SYNC_DATE=08/04/2006

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CPU 1 OF 2-FSB

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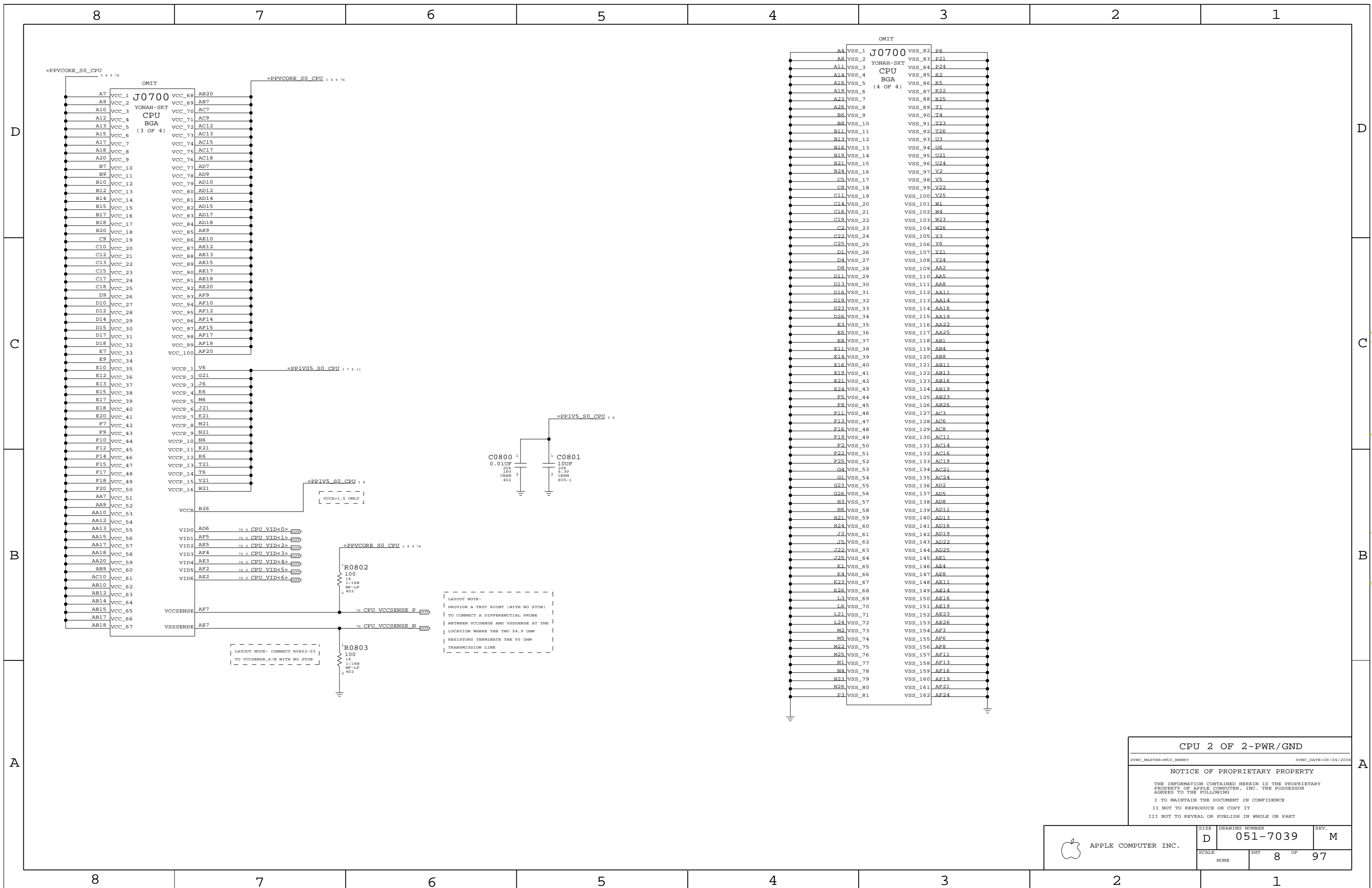
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	SCALE NONE	SHEET 7 OF 97	

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CPU 2 OF 2-PWR/GND

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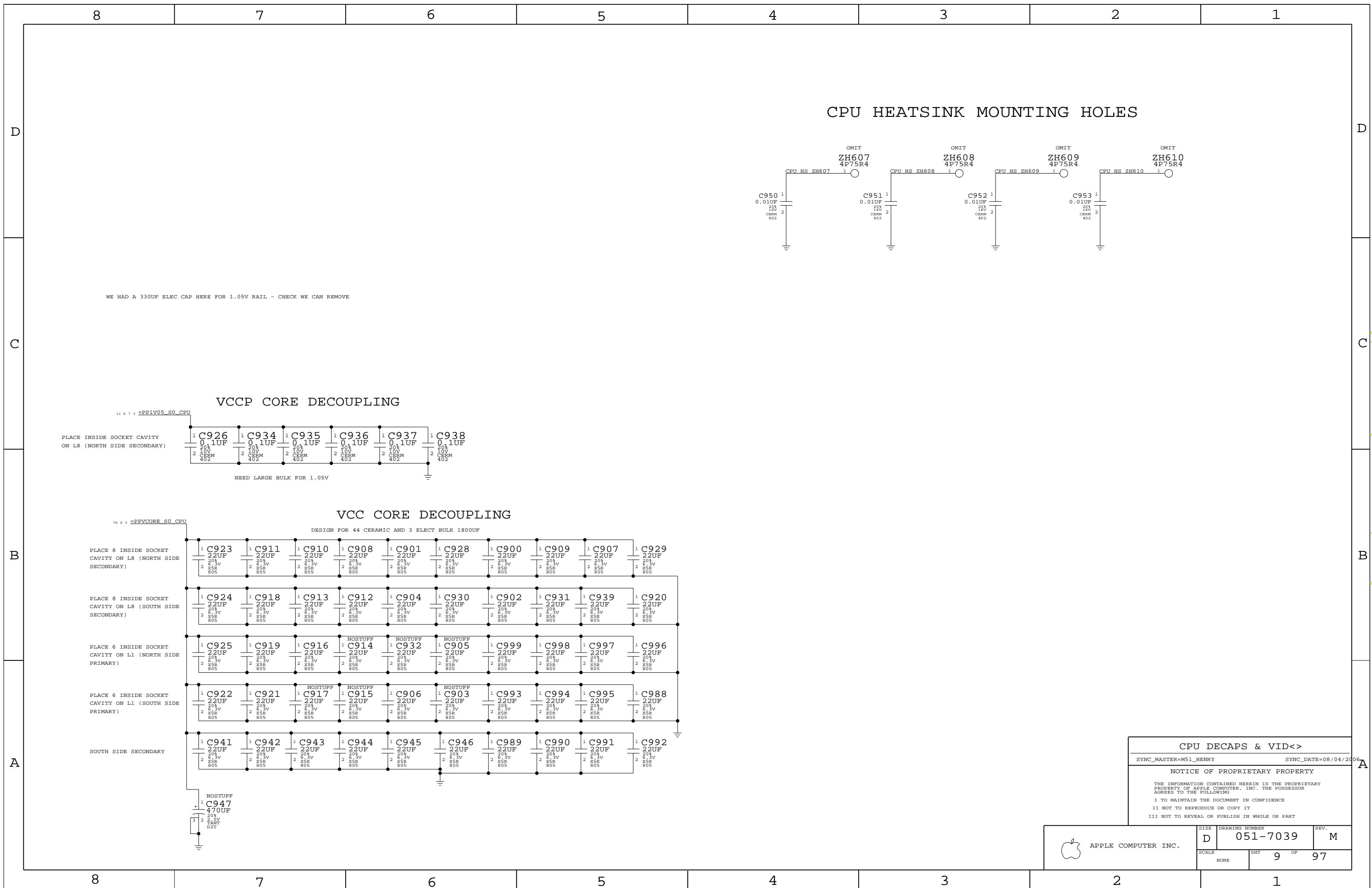
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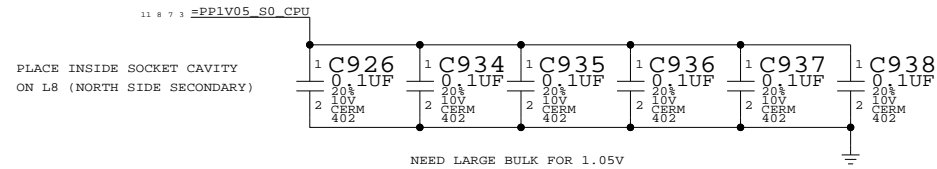
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7039	M
SCALE	SHT	OF	REV.
NONE	8	97	

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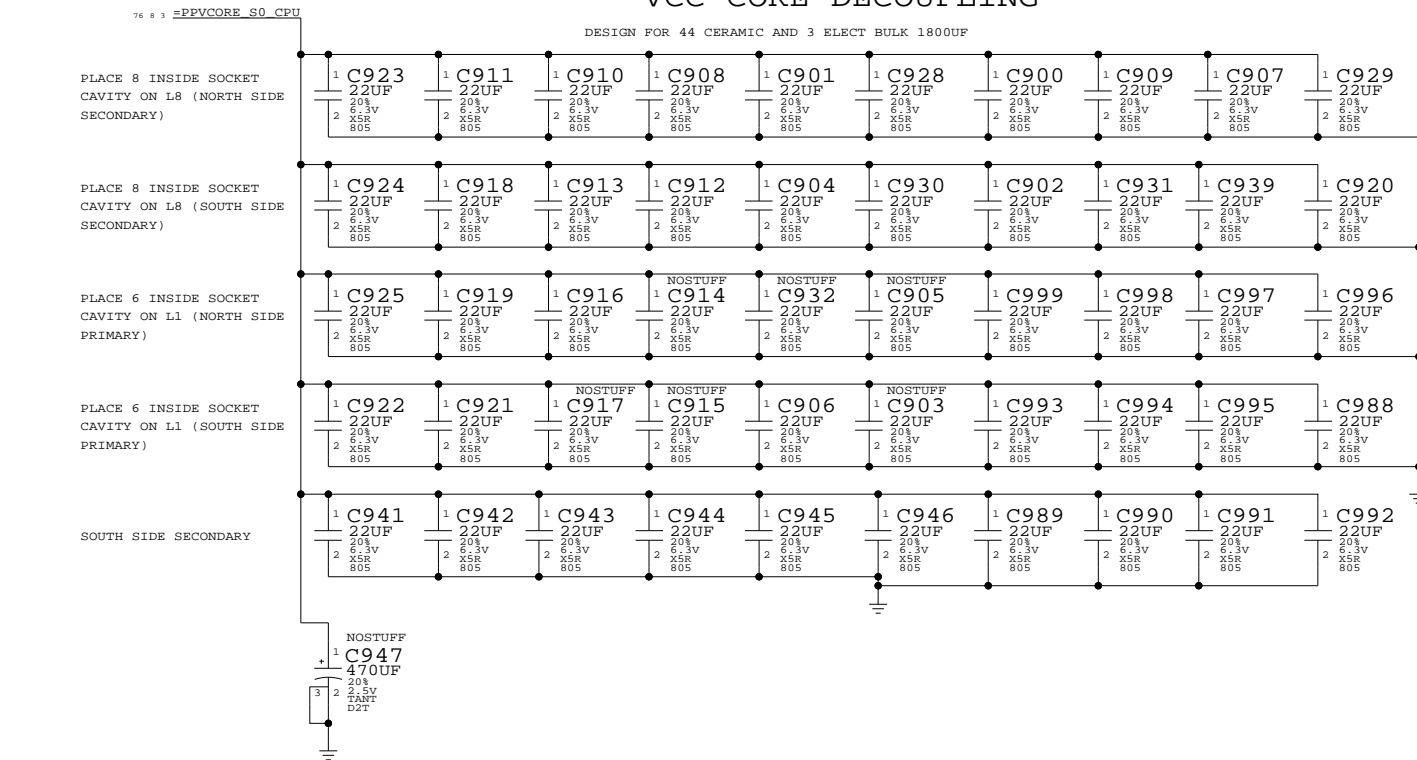
WE HAD A 330UF ELEC CAP HERE FOR 1.05V RAIL - CHECK WE CAN REMOVE

VCCP CORE DECOUPLING

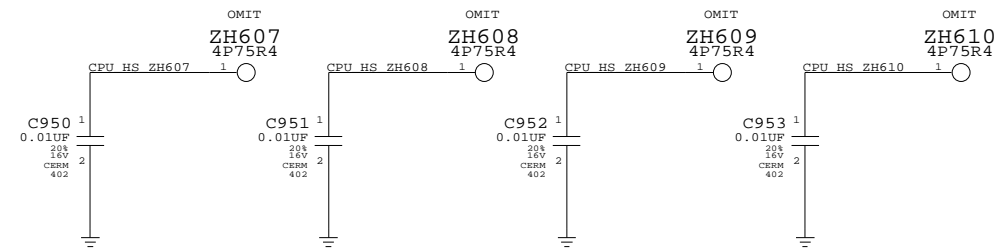


VCC CORE DECOUPLING

DESIGN FOR 44 CERAMIC AND 3 ELECT BULK 1800UF



CPU HEATSINK MOUNTING HOLES



CPU DECAPS & VID<>

SYNC_MASTER=M51_HENRY SYNC_DATE=08/04/2006

NOTICE OF PROPRIETARY PROPERTY

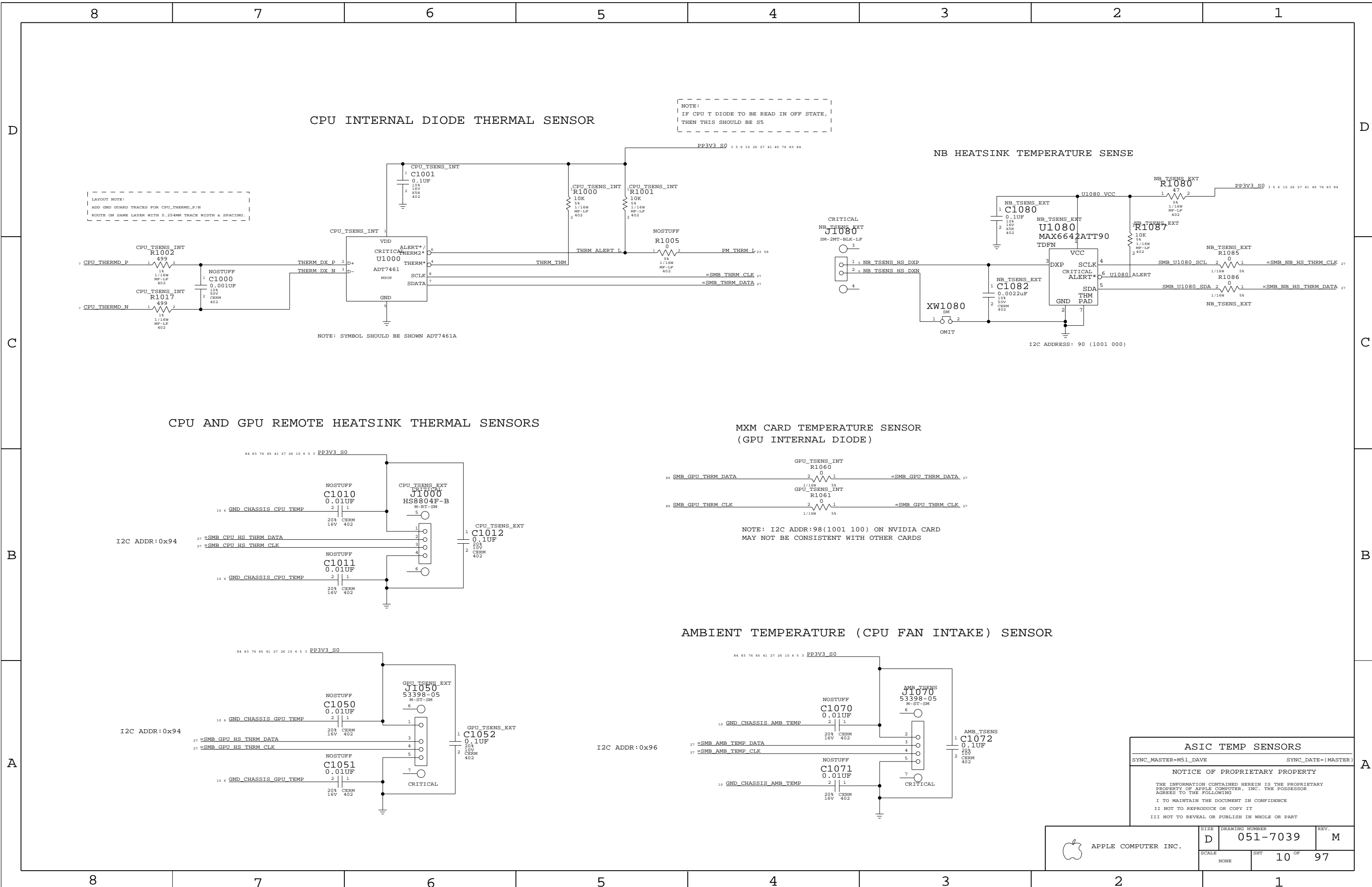
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NONE			



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ASIC TEMP SENSORS

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

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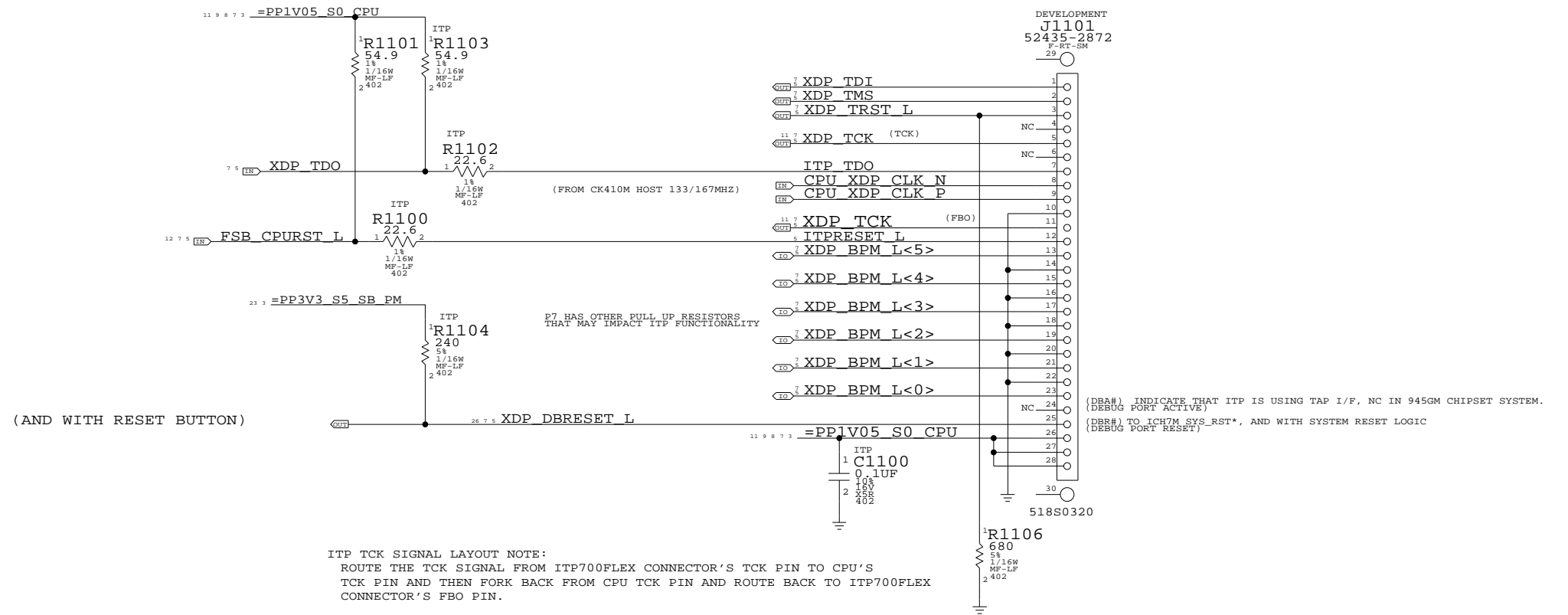
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	D	051-7039	M
SCALE	SHT	10 OF 97	
NONE			

CPU ITP700FLEX DEBUG SUPPORT



CPU ITP700FLEX DEBUG
 SYNC_MASTER=M50_HENRY SYNC_DATE=08/04/2006

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SCALE	SHT	11 OF	97
NONE			

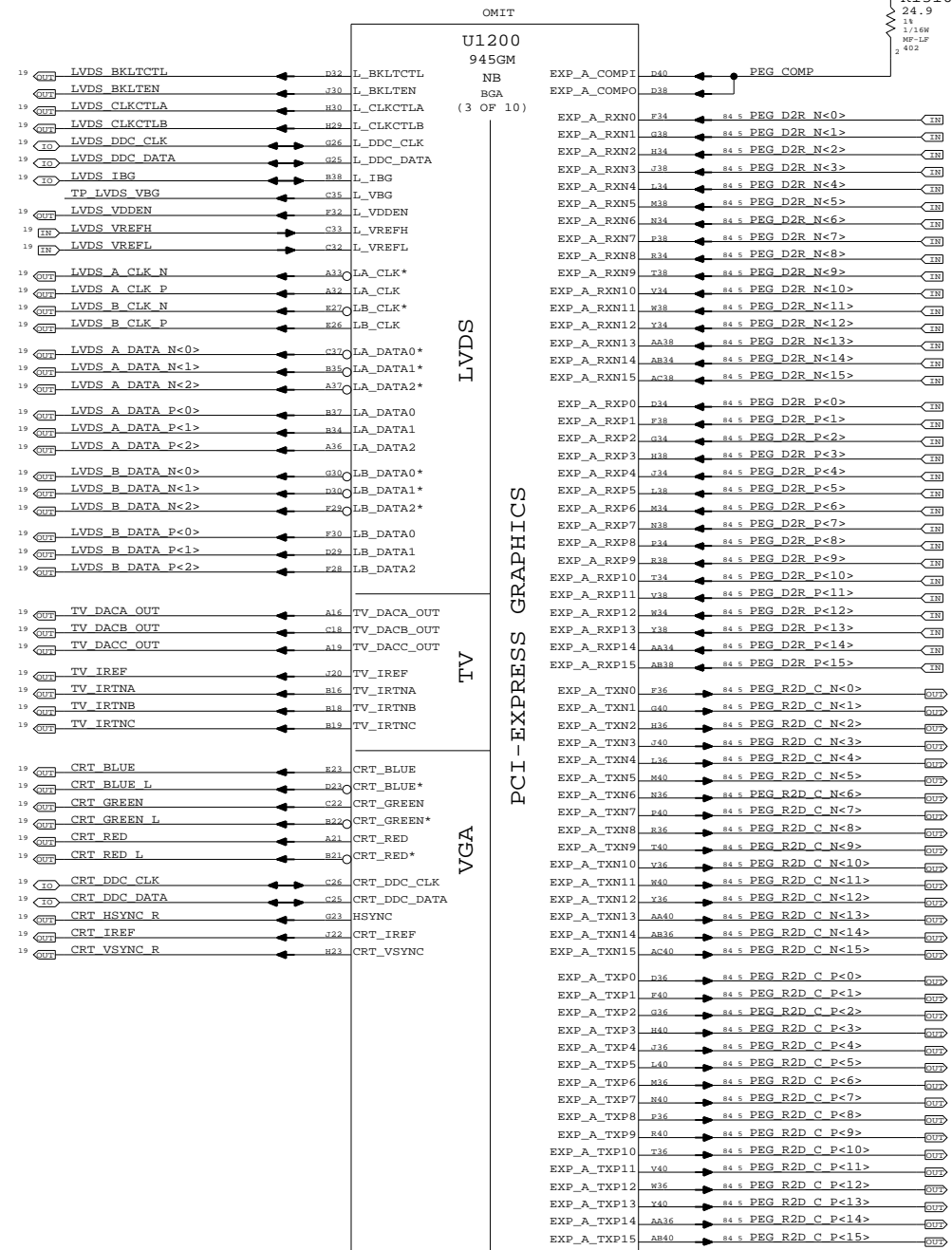
LVDS Disable
 Can leave all signals NC if LVDS is not implemented
 Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
 VCCD_LVDS must remain powered with proper decoupling.
 Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:
 Composite: DACA only
 S-Video: DACB & DACC only
 Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit
 filtering components. Unused DAC outputs should
 connect to GND through 75-ohm resistors.

TV-Out Disable
 Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
 Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
 VCCA_TVVBG to 1.5V power rail. Tie VSSA_TVVBG to GND.

CRT Disable
 Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
 HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
 rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.



SDVO Alternate Function

SDVO_TVCLKIN#
 SDVO_INT#
 SDVO_FLDSTALL#

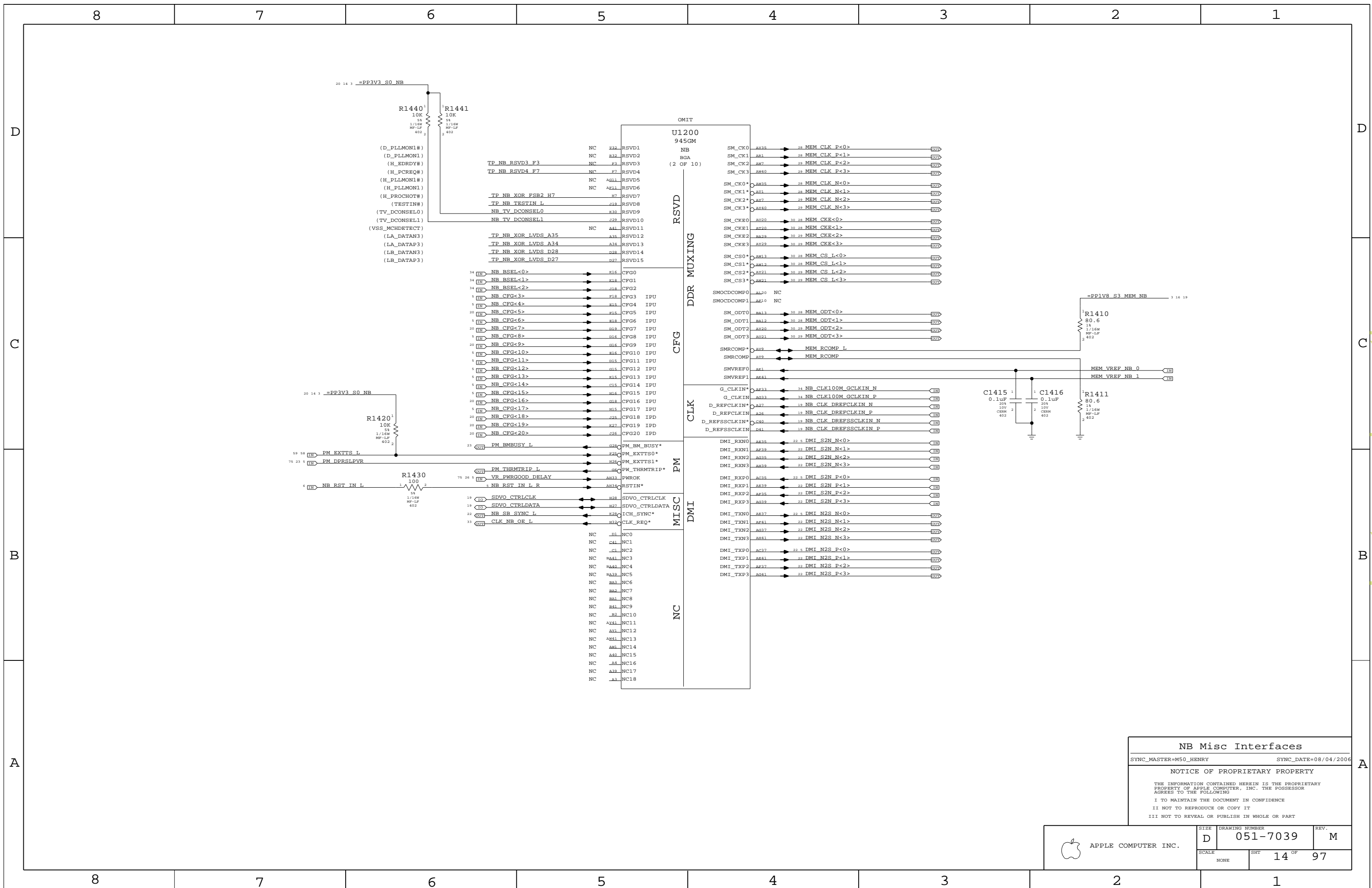
SDVO_TVCLKIN
 SDVO_INT
 SDVO_FLDSTALL

SDVOB_RED#
 SDVOB_GREEN#
 SDVOB_BLUE#
 SDVOB_CLKN
 SDVOC_RED#
 SDVOC_GREEN#
 SDVOC_BLUE#
 SDVOC_CLKN

SDVOB_RED
 SDVOB_GREEN
 SDVOB_BLUE
 SDVOB_CLKP
 SDVOC_RED
 SDVOC_GREEN
 SDVOC_BLUE
 SDVOC_CLKP

NB PEG / Video Interfaces
 SYNC_MASTER=M50_HENRY SYNC_DATE=08/04/2006
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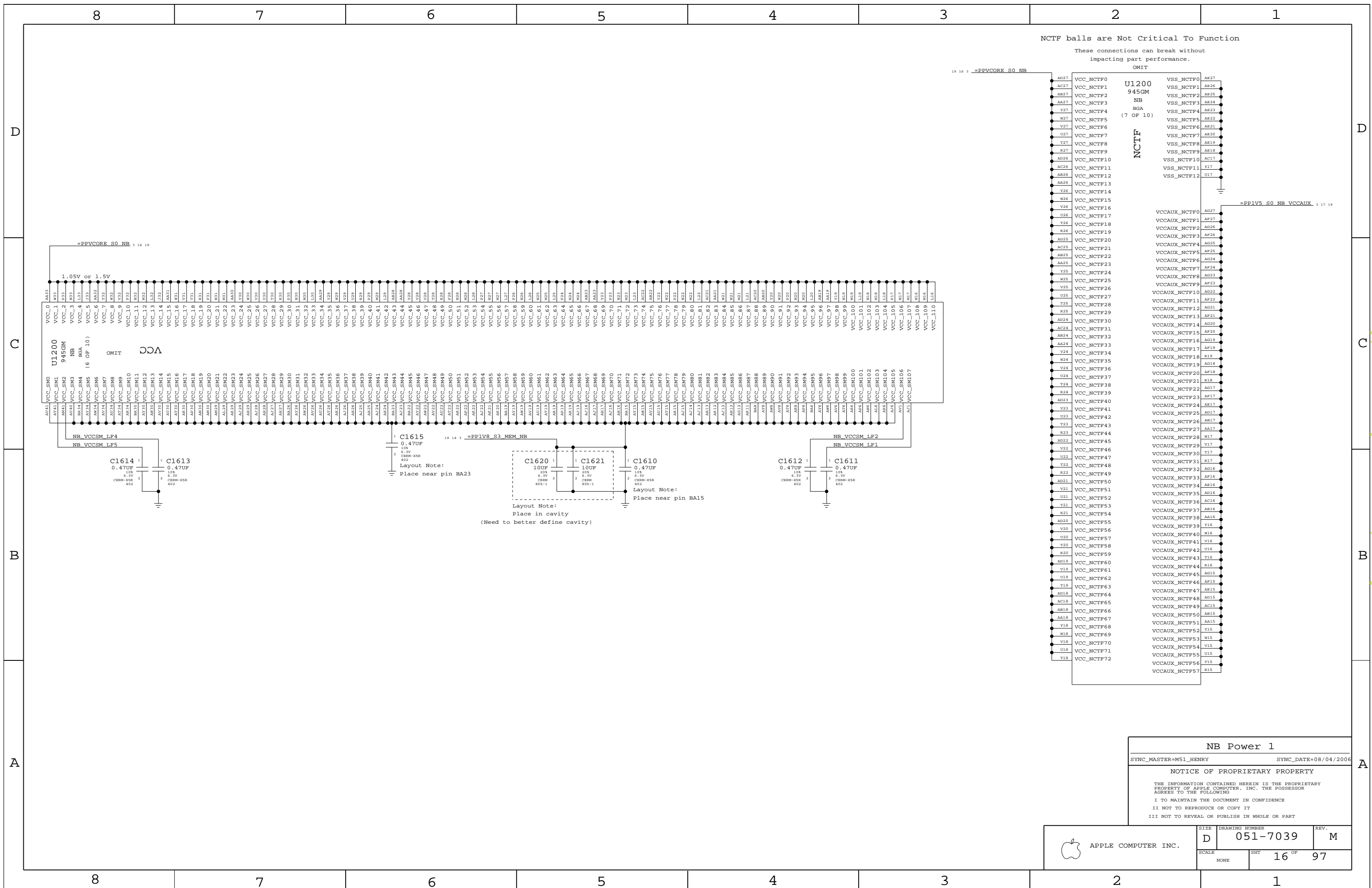
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7039	M
SCALE	SHT	13 OF 97	
NONE			



NB Misc Interfaces
 SYNC_MASTER=M50_HENRY SYNC_DATE=08/04/2006

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	D	051-7039	M
SCALE	SHT	14 OF 97	
NONE			



NCTF balls are Not Critical To Function
 These connections can break without impacting part performance.
 OMIT

U1200
 945GM
 NB
 BGA
 (7 OF 10)
 NCTF

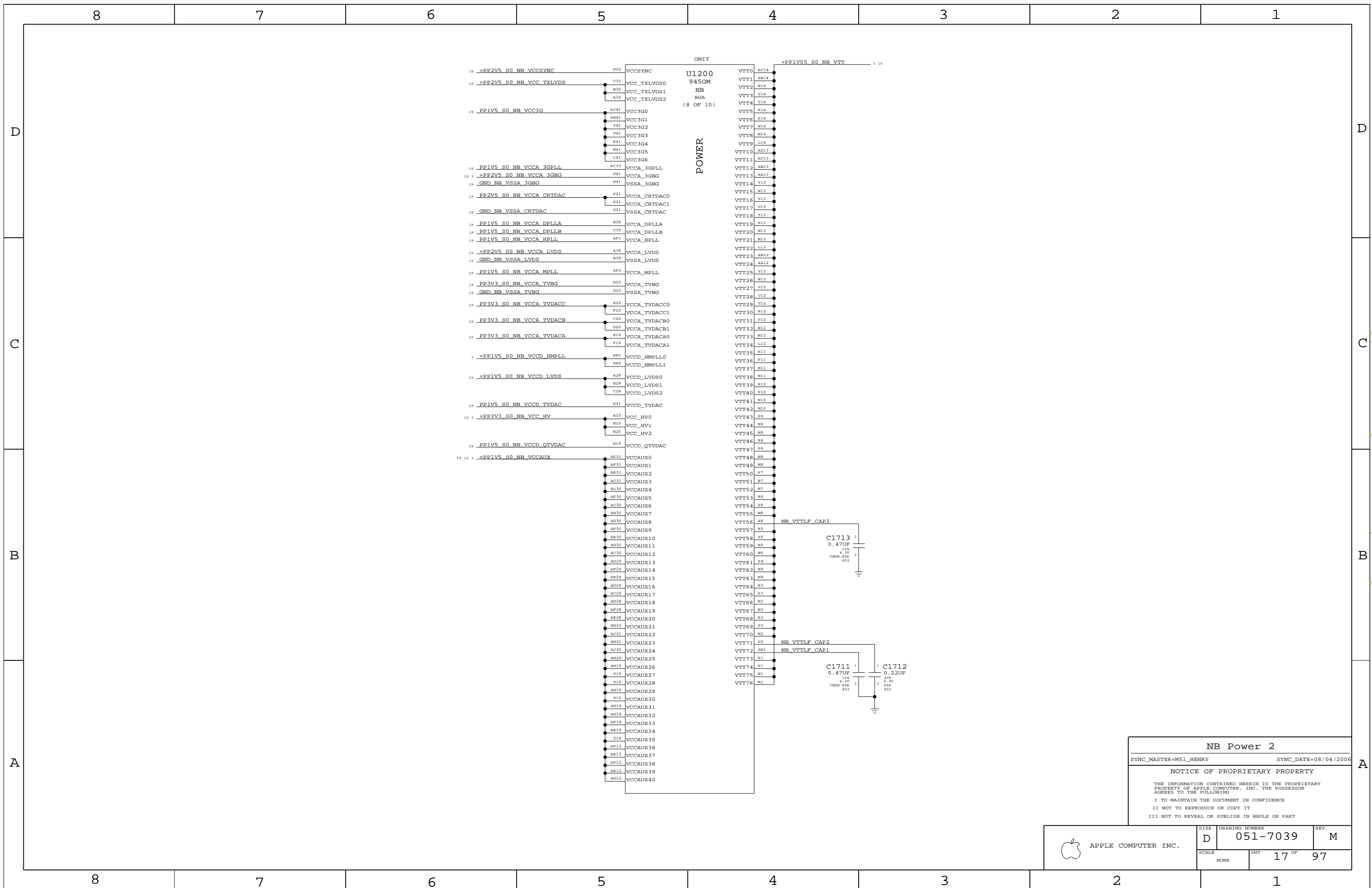
VSS_NCTF0
 VSS_NCTF1
 VSS_NCTF2
 VSS_NCTF3
 VSS_NCTF4
 VSS_NCTF5
 VSS_NCTF6
 VSS_NCTF7
 VSS_NCTF8
 VSS_NCTF9
 VSS_NCTF10
 VSS_NCTF11
 VSS_NCTF12
 VCCAUX_NCTF0
 VCCAUX_NCTF1
 VCCAUX_NCTF2
 VCCAUX_NCTF3
 VCCAUX_NCTF4
 VCCAUX_NCTF5
 VCCAUX_NCTF6
 VCCAUX_NCTF7
 VCCAUX_NCTF8
 VCCAUX_NCTF9
 VCCAUX_NCTF10
 VCCAUX_NCTF11
 VCCAUX_NCTF12
 VCCAUX_NCTF13
 VCCAUX_NCTF14
 VCCAUX_NCTF15
 VCCAUX_NCTF16
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 VCCAUX_NCTF18
 VCCAUX_NCTF19
 VCCAUX_NCTF20
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 VCCAUX_NCTF28
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 VCCAUX_NCTF30
 VCCAUX_NCTF31
 VCCAUX_NCTF32
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 VCCAUX_NCTF34
 VCCAUX_NCTF35
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 VCCAUX_NCTF40
 VCCAUX_NCTF41
 VCCAUX_NCTF42
 VCCAUX_NCTF43
 VCCAUX_NCTF44
 VCCAUX_NCTF45
 VCCAUX_NCTF46
 VCCAUX_NCTF47
 VCCAUX_NCTF48
 VCCAUX_NCTF49
 VCCAUX_NCTF50
 VCCAUX_NCTF51
 VCCAUX_NCTF52
 VCCAUX_NCTF53
 VCCAUX_NCTF54
 VCCAUX_NCTF55
 VCCAUX_NCTF56
 VCCAUX_NCTF57

NB Power 1
 SYNC_MASTER=M51_HENRY SYNC_DATE=08/04/2006

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SCALE	SHT	16 OF	97
NONE			

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NB Power 2

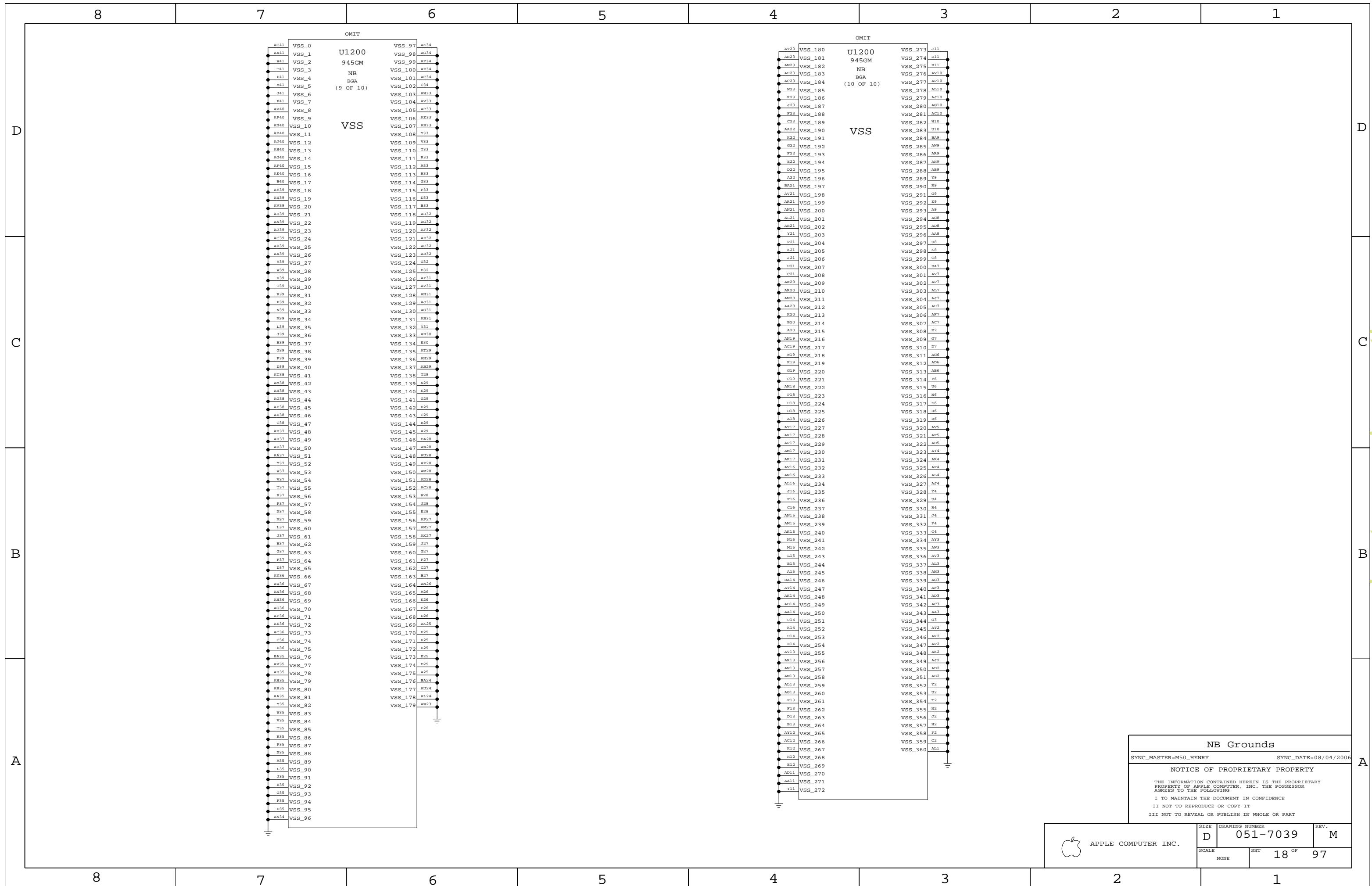
SYNC_MASTER=M51_HENRY SYNC_DATE=08/04/2006

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	SCALE NONE	SHEET 17 OF 97	



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NB Grounds

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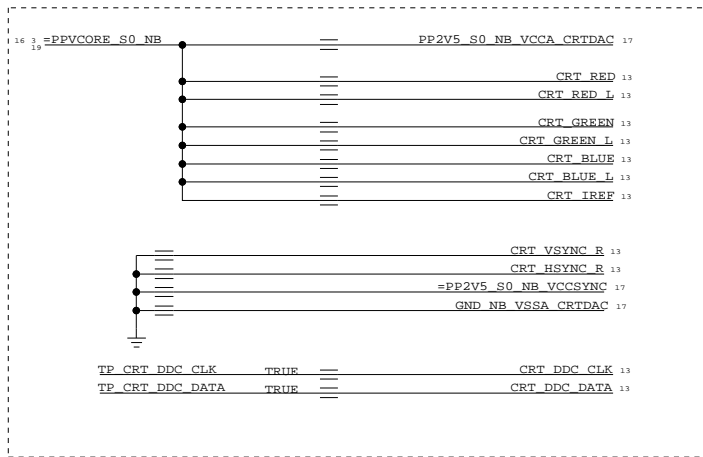
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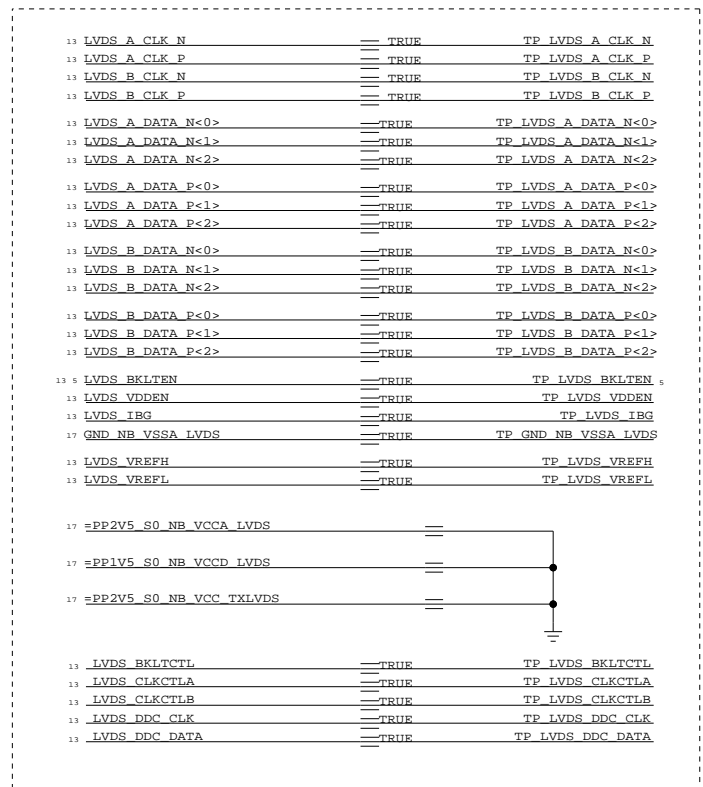
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7039	REV. M
	SCALE NONE	SHEET 18 OF 97	

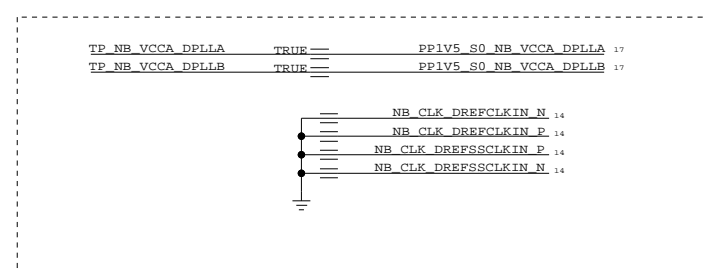
TVOUT DISABLE



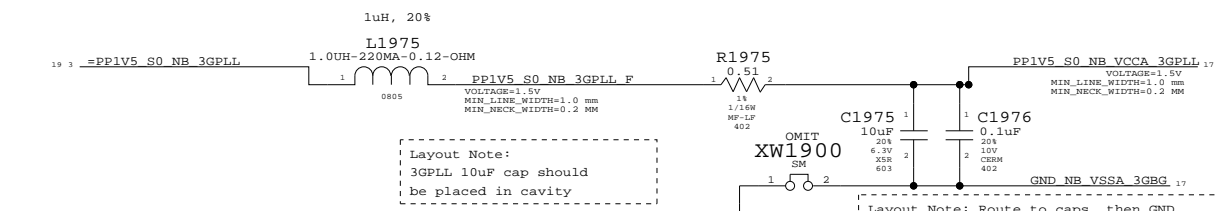
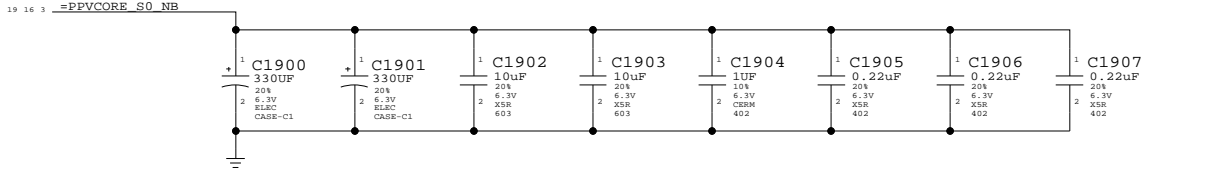
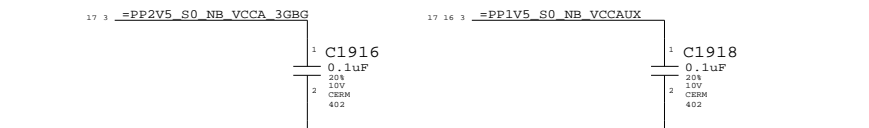
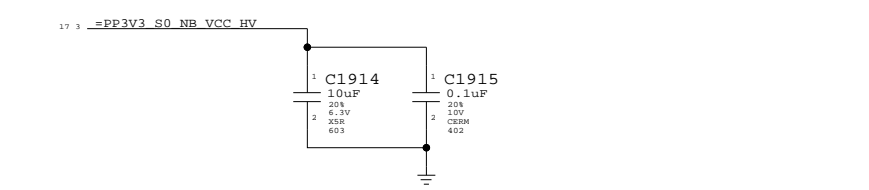
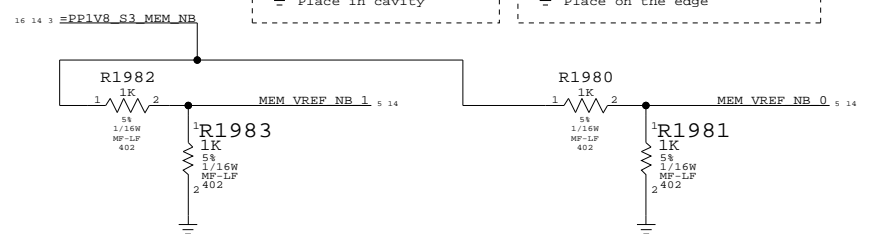
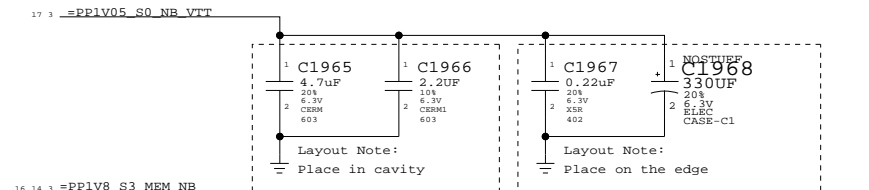
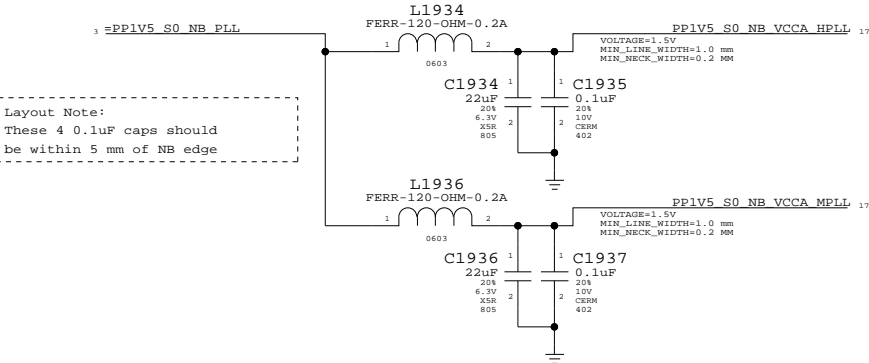
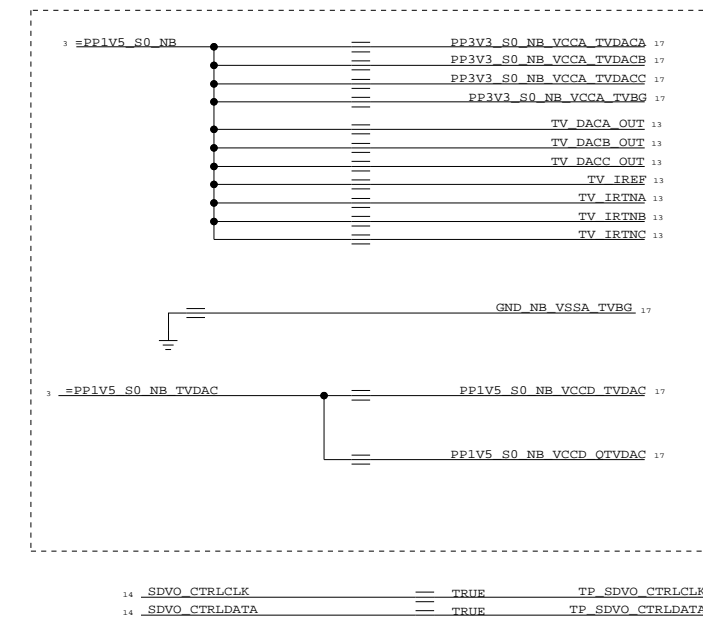
LVDS DISABLE



DISPLAY DISABLE



TVOUT DISABLE



NB (GM) Decoupling

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

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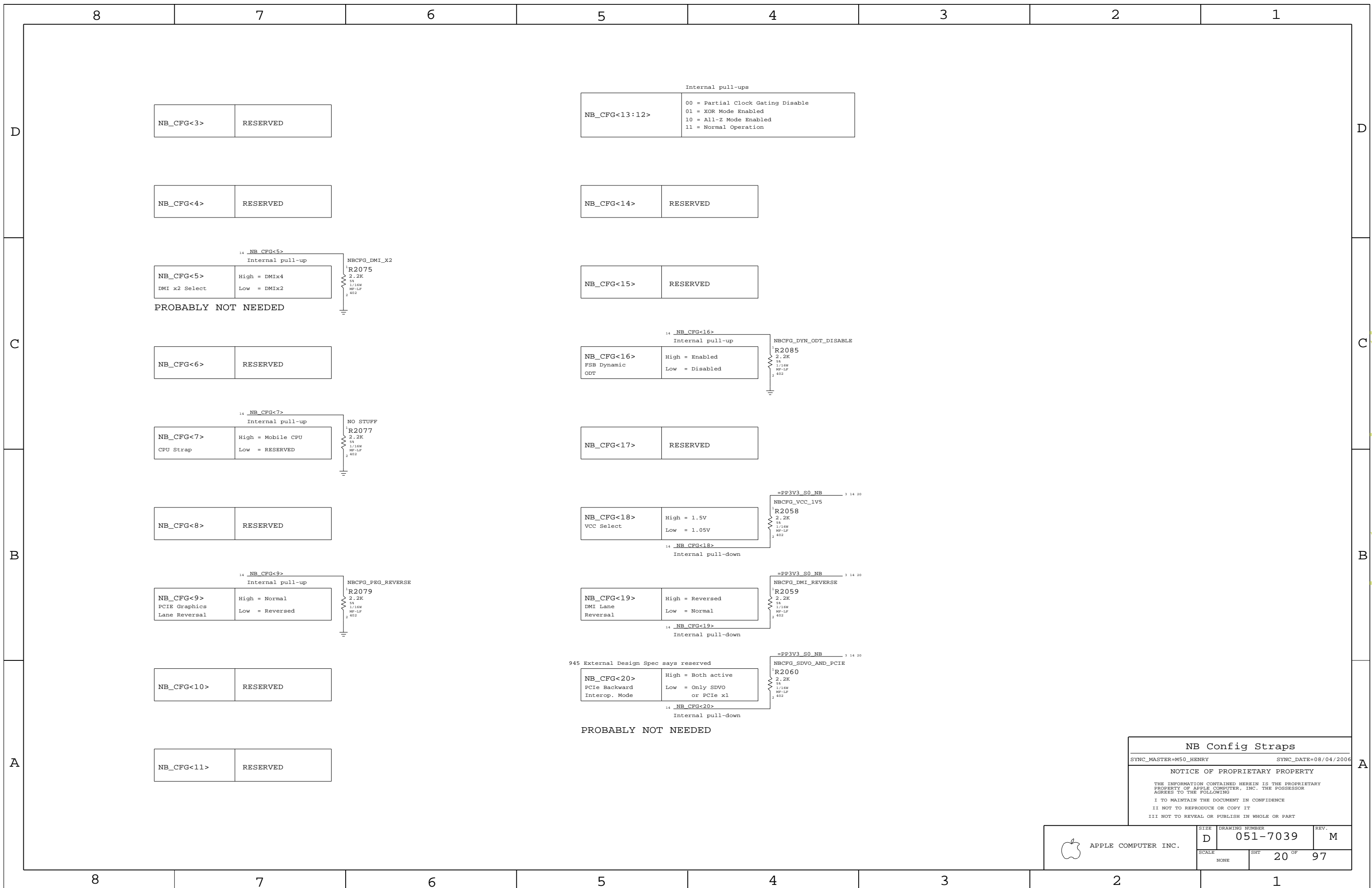
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	D	051-7039	M
SCALE	SHT	19 OF 97	
NONE			



Internal pull-ups

NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation
---------------	--

NB_CFG<3>	RESERVED
-----------	----------

NB_CFG<14>	RESERVED
------------	----------

NB_CFG<4>	RESERVED
-----------	----------

14 NB_CFG<5>
Internal pull-up

NB_CFG<5>	High = DMIX4 DMI x2 Select Low = DMIX2
-----------	--

PROBABLY NOT NEEDED

NBCFG_DMI_X2
R2075
2.2K
5%
1/16W
MF-LP
2 402

NB_CFG<15>	RESERVED
------------	----------

NB_CFG<6>	RESERVED
-----------	----------

14 NB_CFG<16>
Internal pull-up

NB_CFG<16>	High = Enabled FSB Dynamic ODT Low = Disabled
------------	--

NBCFG_DYN_ODT_DISABLE
R2085
2.2K
5%
1/16W
MF-LP
2 402

14 NB_CFG<7>
Internal pull-up

NB_CFG<7>	High = Mobile CPU CPU Strap Low = RESERVED
-----------	--

NO STUFF
R2077
2.2K
5%
1/16W
MF-LP
2 402

NB_CFG<17>	RESERVED
------------	----------

NB_CFG<8>	RESERVED
-----------	----------

=PP3V3_S0_NB 3 14 20

NB_CFG<18>	High = 1.5V VCC Select Low = 1.05V
------------	--

NBCFG_VCC_LV5
R2058
2.2K
5%
1/16W
MF-LP
2 402

14 NB_CFG<18>
Internal pull-down

14 NB_CFG<9>
Internal pull-up

NB_CFG<9>	High = Normal PCIe Graphics Lane Reversal Low = Reversed
-----------	---

NBCFG_PEG_REVERSE
R2079
2.2K
5%
1/16W
MF-LP
2 402

=PP3V3_S0_NB 3 14 20

NB_CFG<19>	High = Reversed DMI Lane Reversal Low = Normal
------------	---

NBCFG_DMI_REVERSE
R2059
2.2K
5%
1/16W
MF-LP
2 402

14 NB_CFG<19>
Internal pull-down

NB_CFG<10>	RESERVED
------------	----------

945 External Design Spec says reserved

NB_CFG<20>	High = Both active PCIe Backward Interop. Mode Low = Only SDVO or PCIe x1
------------	---

=PP3V3_S0_NB 3 14 20
NBCFG_SDVO_AND_PCIE
R2060
2.2K
5%
1/16W
MF-LP
2 402

14 NB_CFG<20>
Internal pull-down

NB_CFG<11>	RESERVED
------------	----------

PROBABLY NOT NEEDED

NB Config Straps

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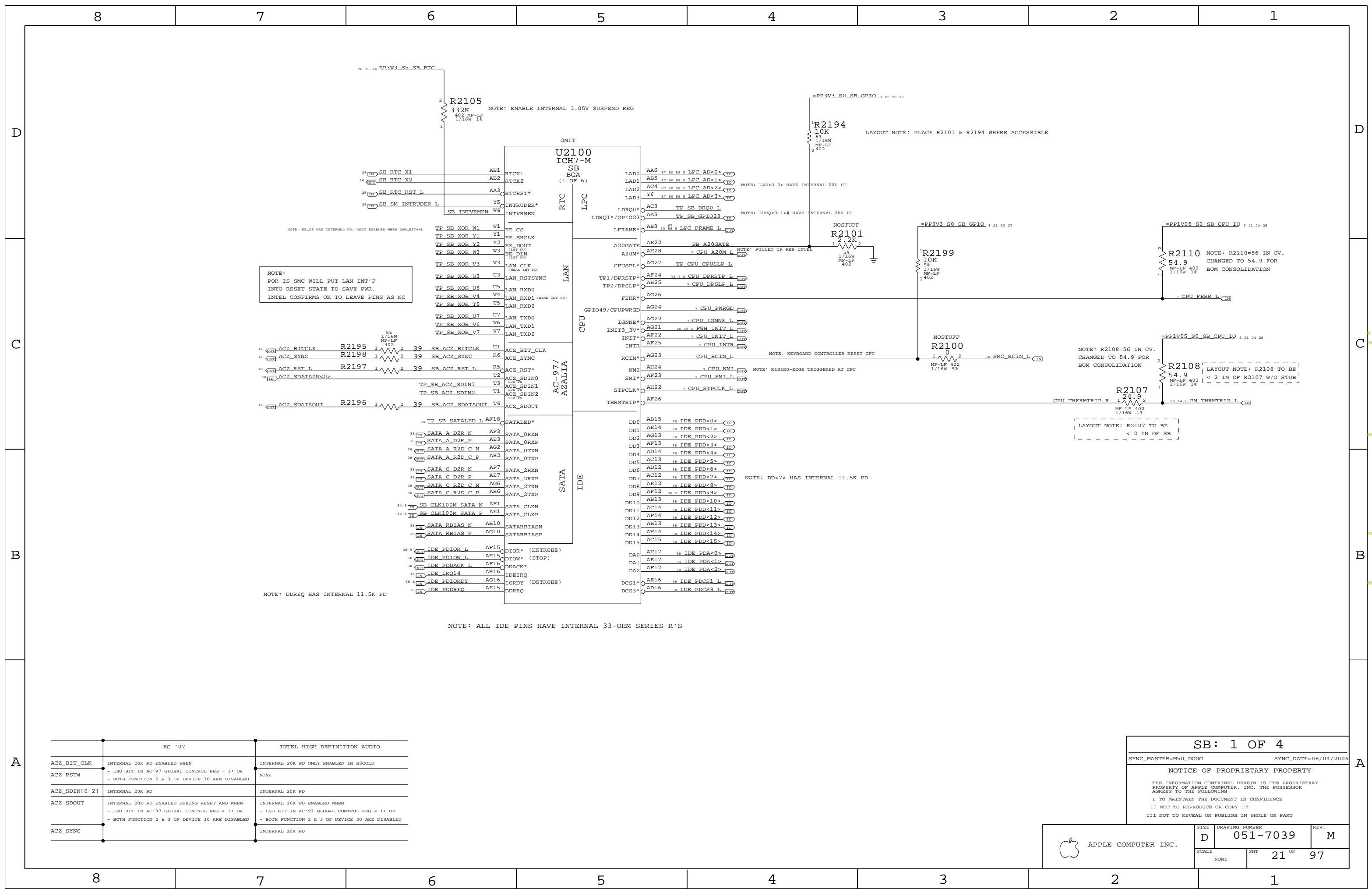
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SCALE	SHT	20 OF 97	
NONE			

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NOTE:
 POR IS SMC WILL PUT LAN INT'F
 INTO RESET STATE TO SAVE PWR.
 INTEL CONFIRMS OK TO LEAVE PINS AS NC

NOTE: DDREQ HAS INTERNAL 11.5K PD

NOTE: ALL IDE PINS HAVE INTERNAL 33-OHM SERIES R'S

AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR
ACZ_RST#	INTERNAL 20K PD ONLY ENABLED IN S3COLD
ACZ_SDIN[0-2]	NONE
ACZ_SDOUT	INTERNAL 20K PD
ACZ_SYNC	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
	INTERNAL 20K PD

SB: 1 OF 4

SYNC_MASTER=M50_DOUG SYNC_DATE=08/04/2006

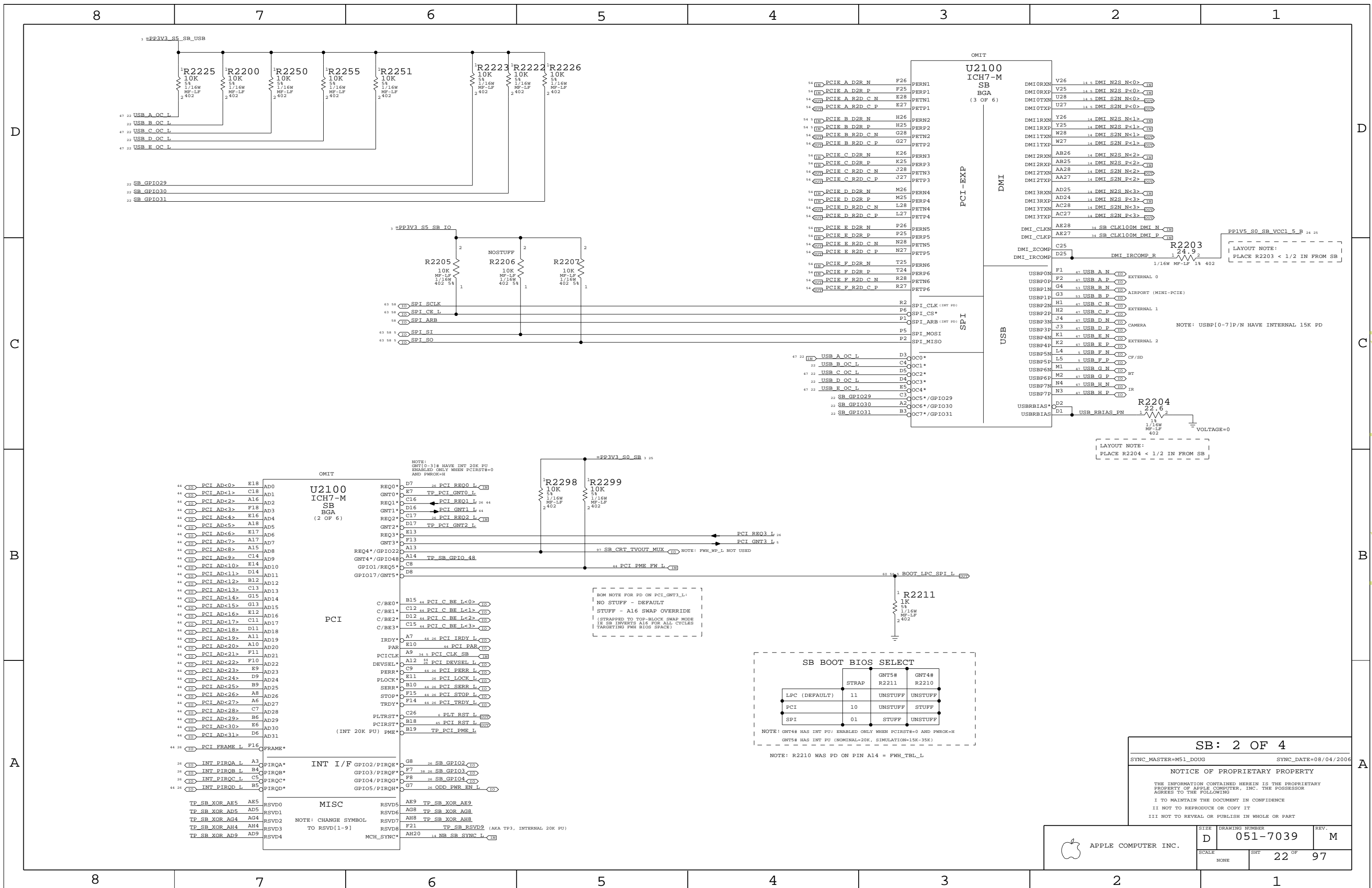
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7039	M
SCALE	SHT	21 OF 97	
NONE			

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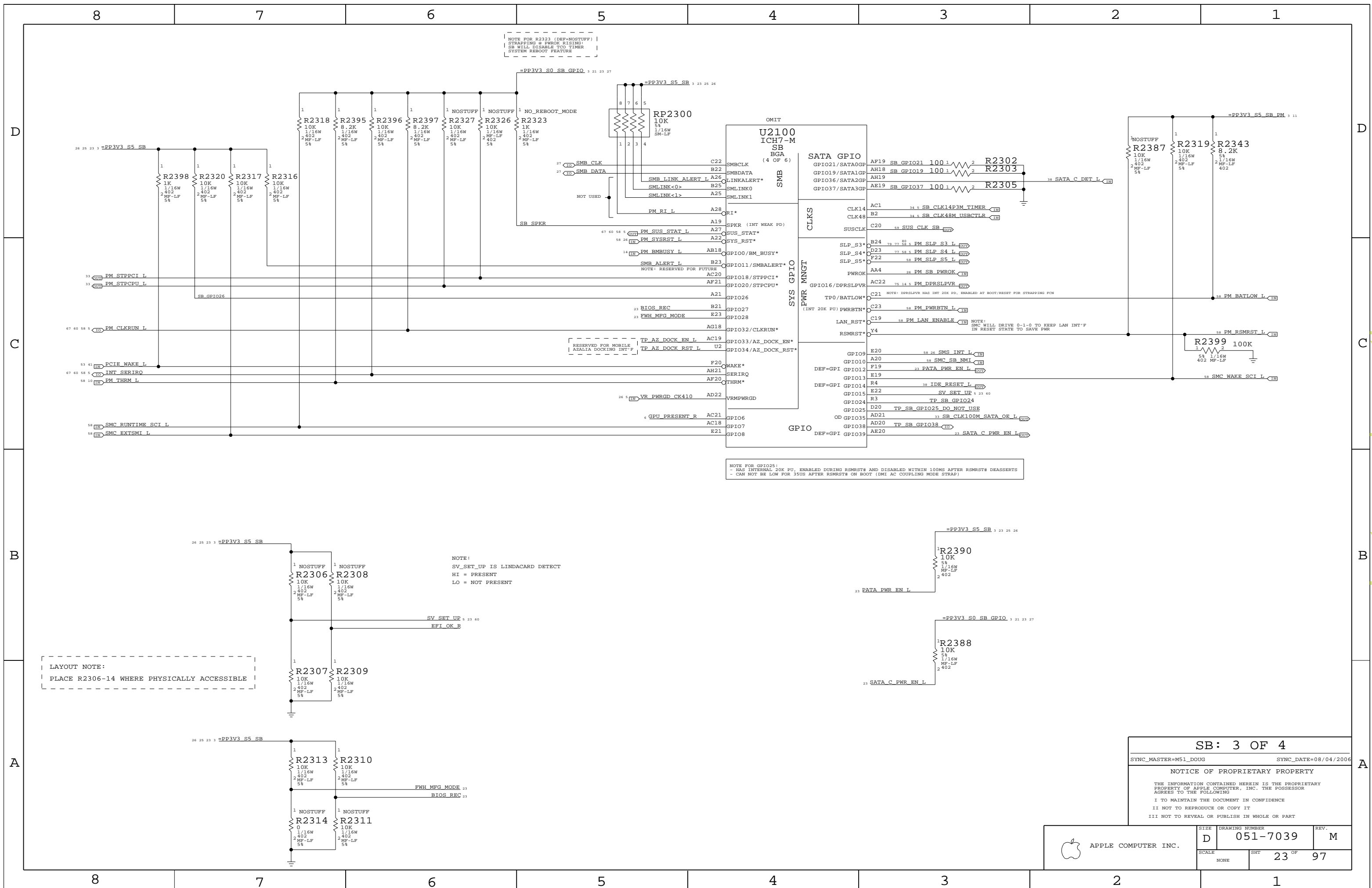
SB: 2 OF 4

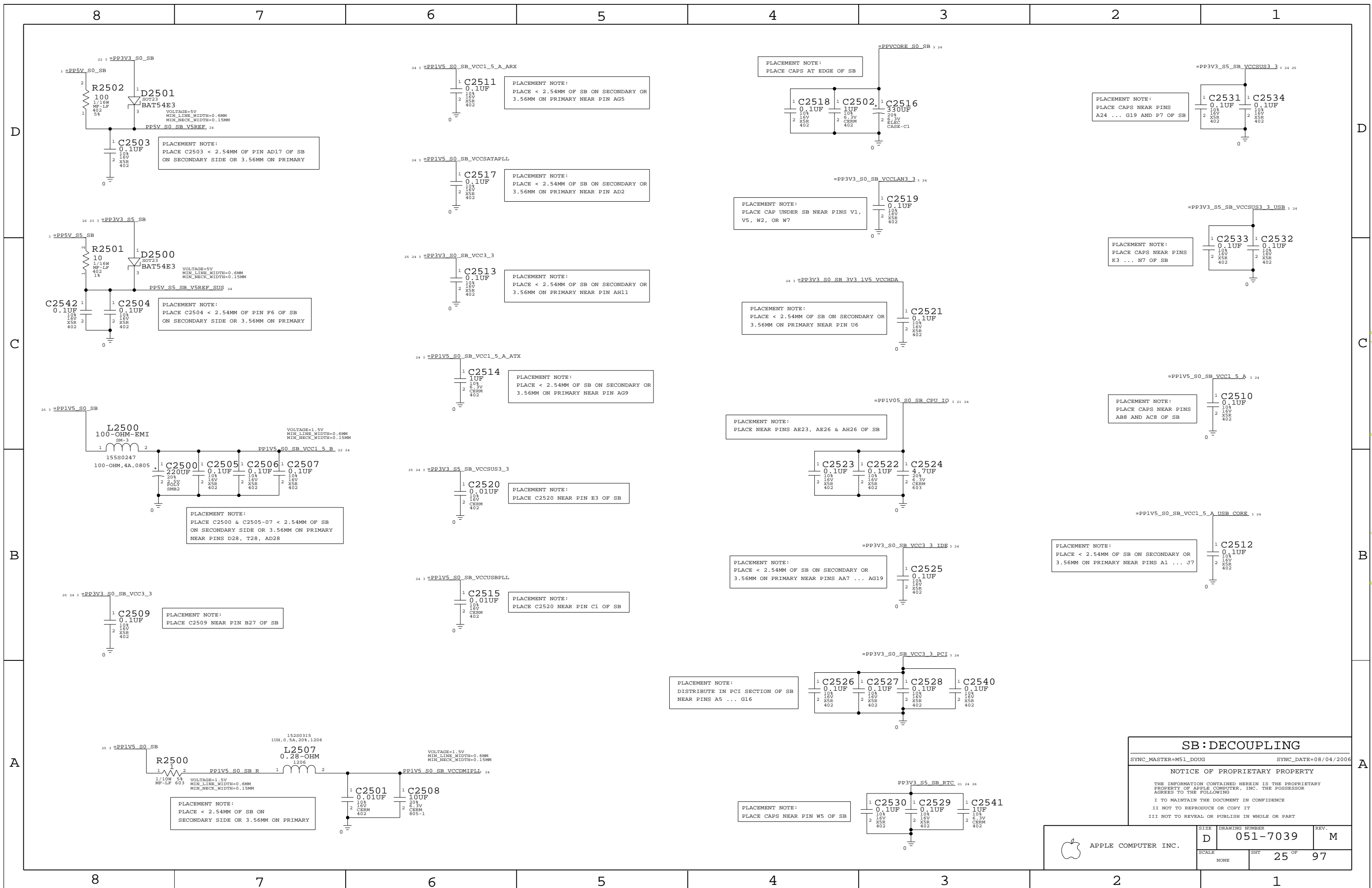
SYNC_MASTER=M51_D0UG SYNC_DATE=08/04/2006

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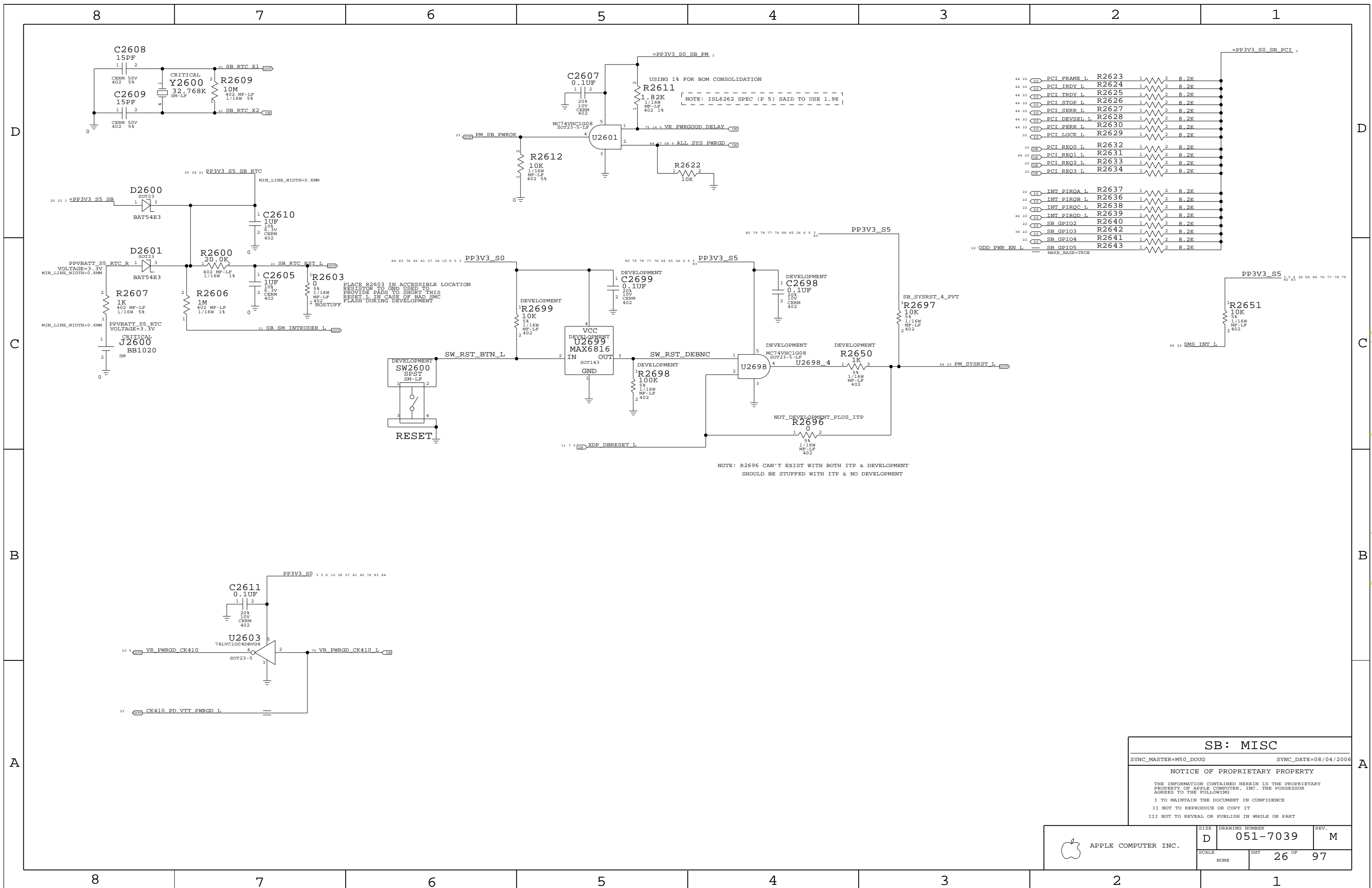
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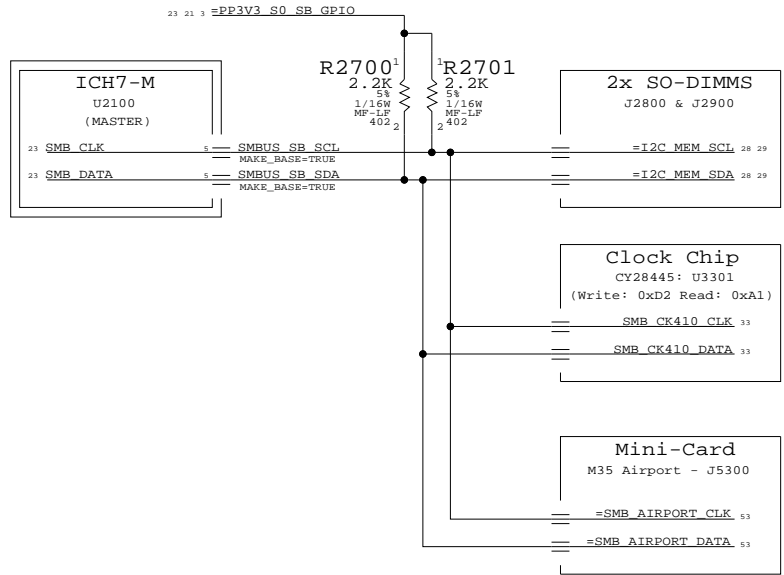


SB: DECOUPLING
 SYNC_MASTER=M51_DOUG SYNC_DATE=08/04/2006
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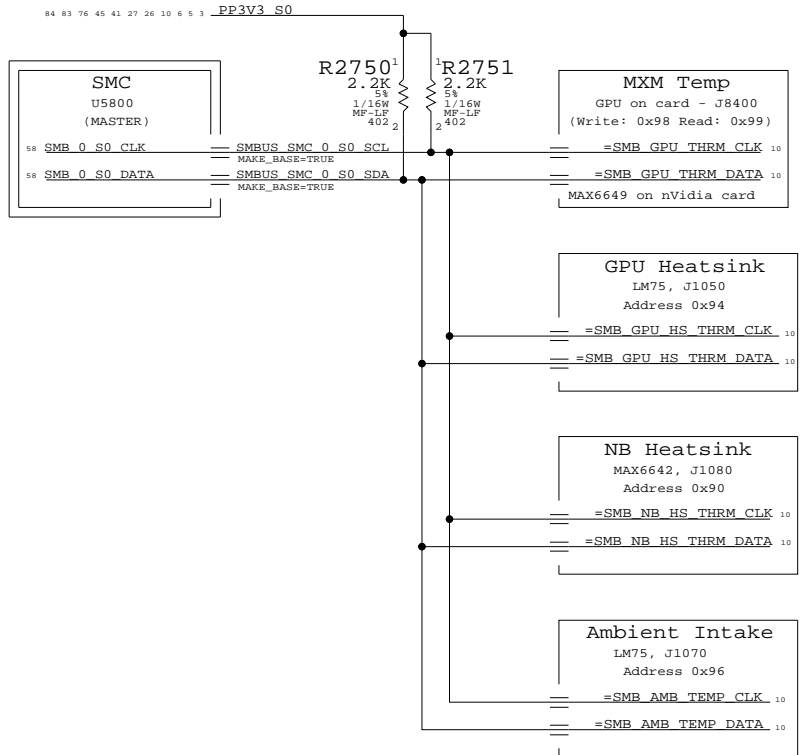
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7039	M
SCALE	SHT	25 OF	97
NONE			



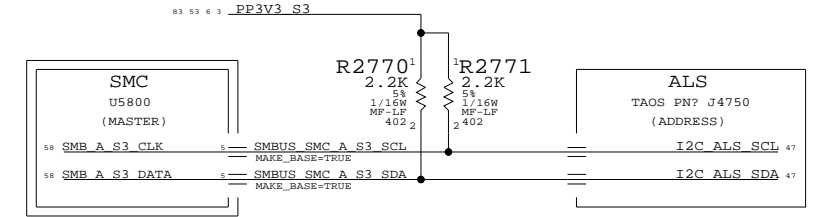
ICH7-M SMBus Connections



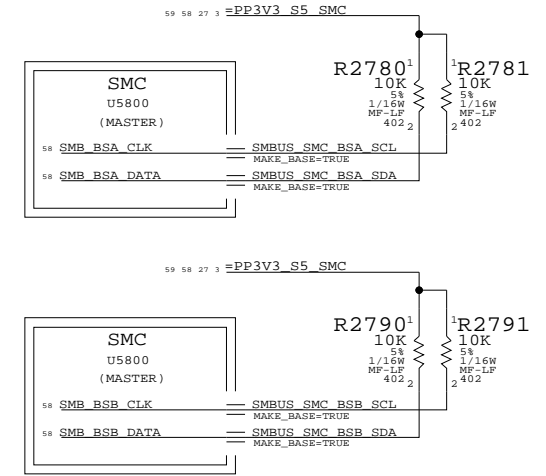
SMC "0" SMBus Connections



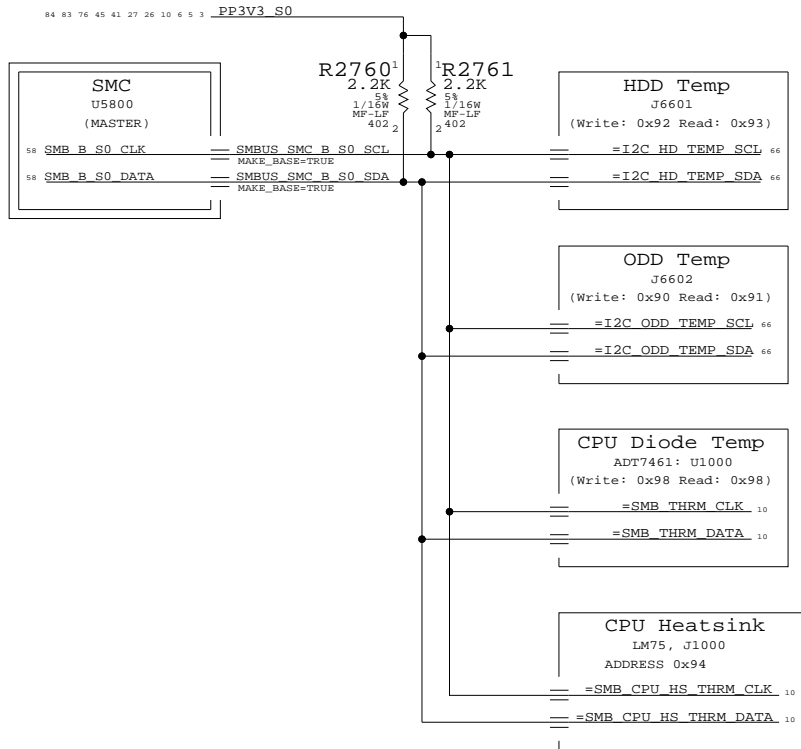
SMC "A" SMBus Connections



Unused SMC "Battery A/B" SMBus



SMC "B" SMBus Connections



M51 SMBus Connections

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7039	M
SCALE	SHT	27 OF 97	
NONE			

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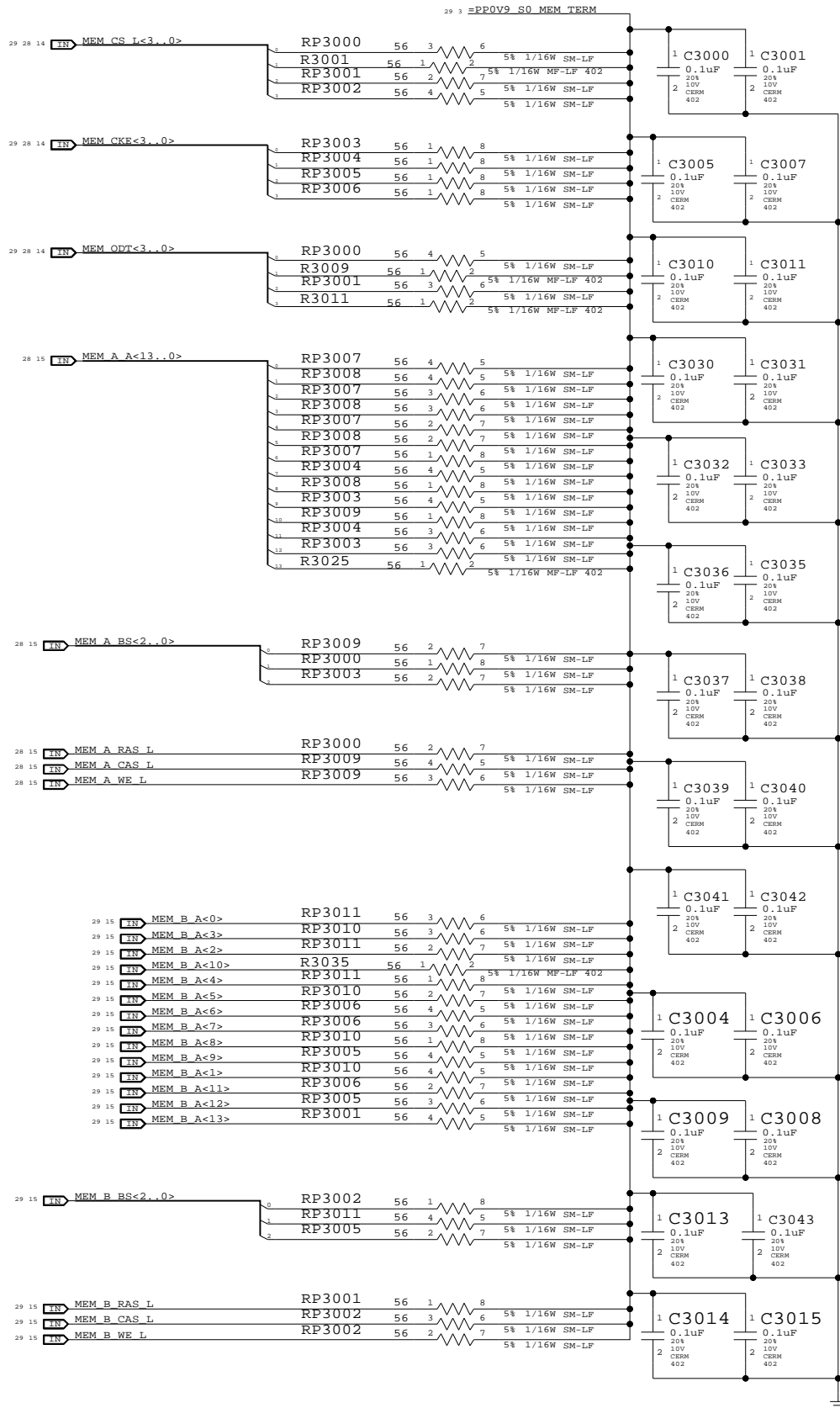
4

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1

One cap for each side of every RPAK, one cap for every two discrete resistors
BOMOPTION shown at the top of each group applies to every part below it



Memory Active Termination

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	D	051-7039	M
SCALE	SHT	OF	
NONE	30	97	

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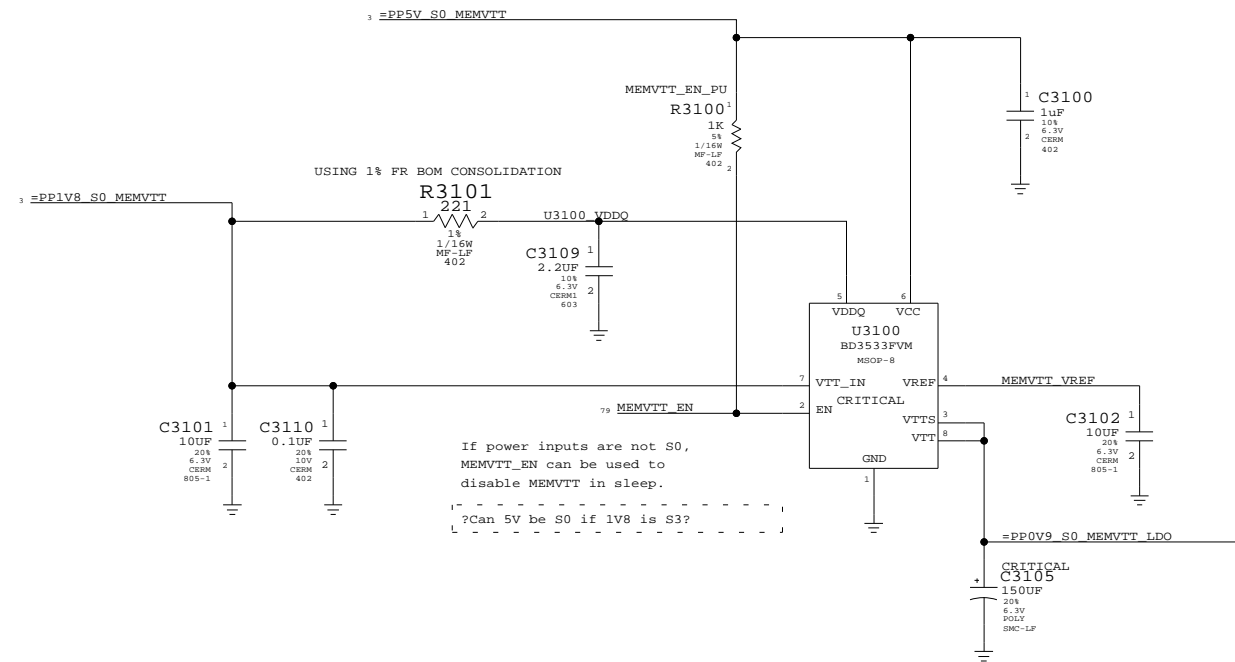
Page Notes

Power aliases required by this page:
 - =PP5V_S0_MEMVTT
 - =PP1V8_S0_MEMVTT
 - =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
 (NONE)

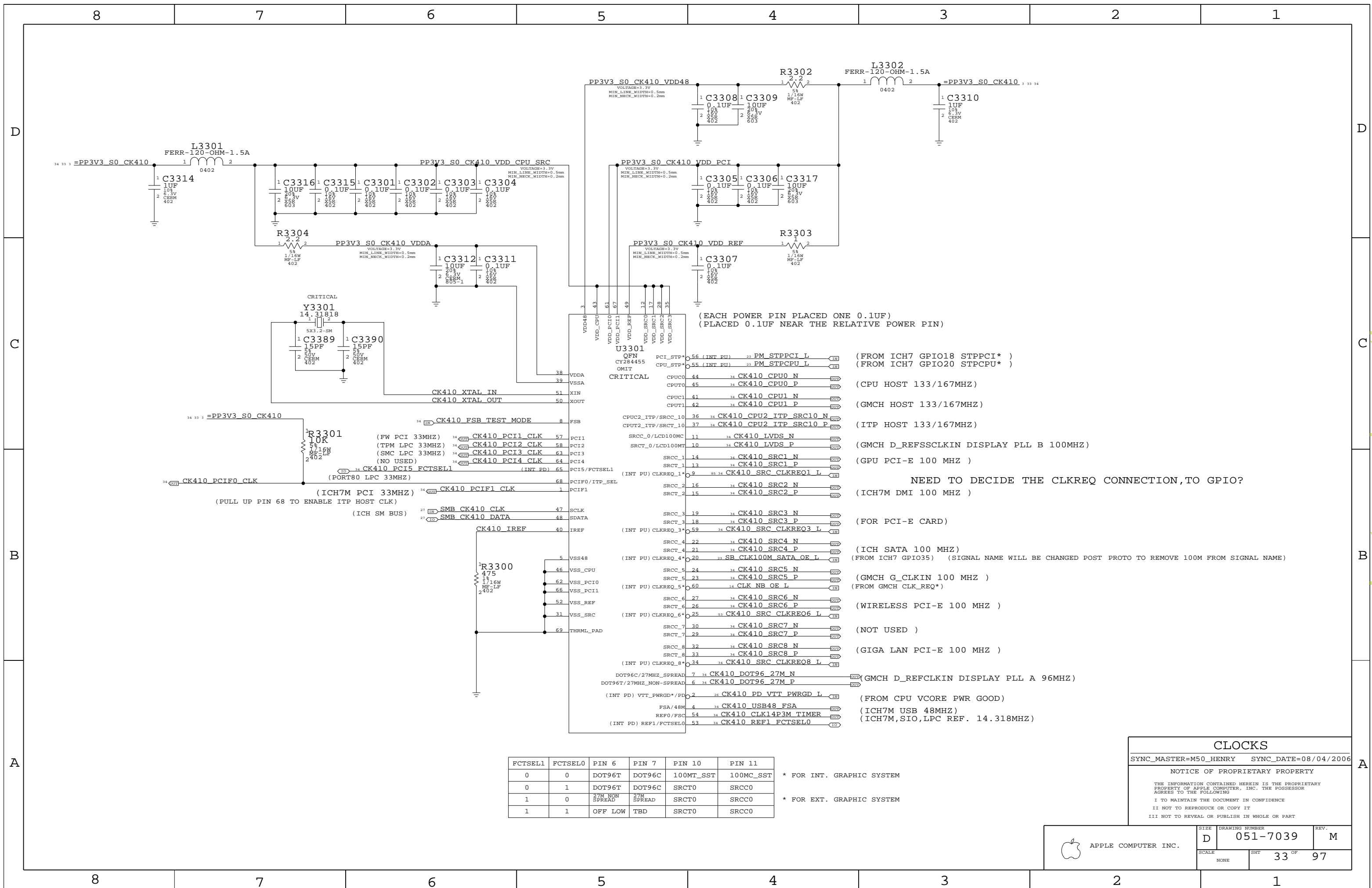
BOM options provided by this page:
 (NONE)

DDR2 Vtt Regulator



Memory Vtt Supply
 SYNC_MASTER=M50_HENRY SYNC_DATE=08/04/2006
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	D	051-7039	M
SCALE	SHT	31 OF 97	
NONE			



FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST
0	1	DOT96T	DOT96C	SRCT0	SRCC0
1	0	27M NON SPREAD	27M SPREAD	SRCT0	SRCC0
1	1	OFF LOW	TBD	SRCT0	SRCC0

* FOR INT. GRAPHIC SYSTEM
 * FOR EXT. GRAPHIC SYSTEM

CLOCKS

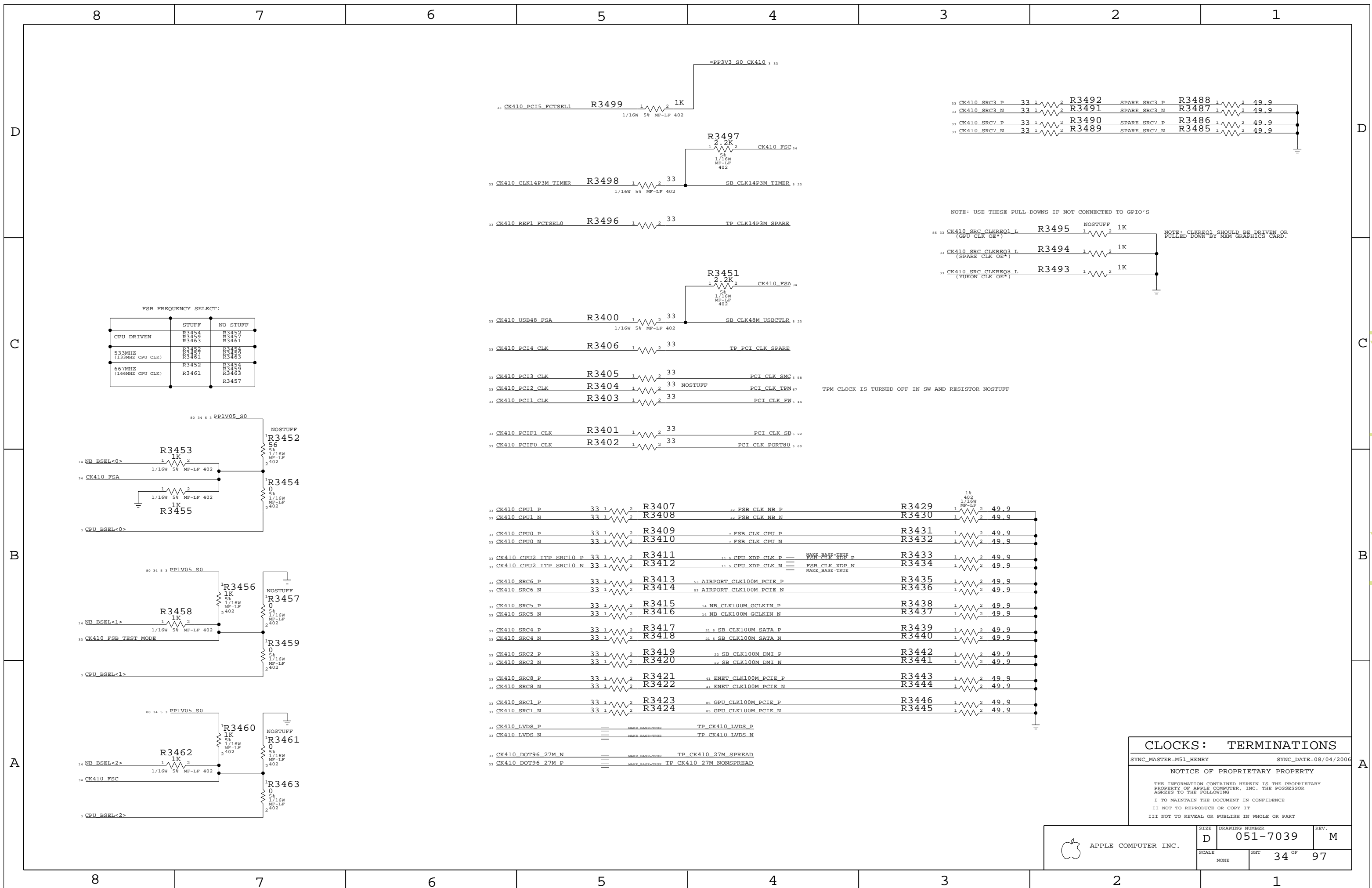
SYNC_MASTER=M50_HENRY SYNC_DATE=08/04/2006

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	D	051-7039	M
SCALE	SHT	33 OF 97	
NONE			



FSB FREQUENCY SELECT:

	STUFF	NO STUFF
CPU DRIVEN	R3452 R3453 R3454 R3455	R3457 R3458 R3459 R3460
533MHZ (133MHZ CPU CLK)	R3452 R3453 R3454 R3455	R3457 R3458 R3459 R3460
667MHZ (166MHZ CPU CLK)	R3452 R3453 R3454 R3455	R3457 R3458 R3459 R3460

CLOCKS: TERMINATIONS

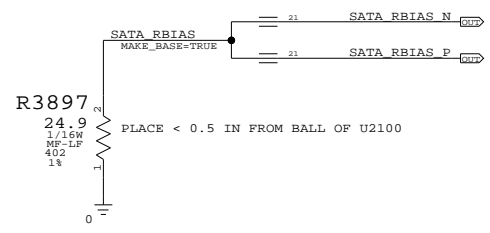
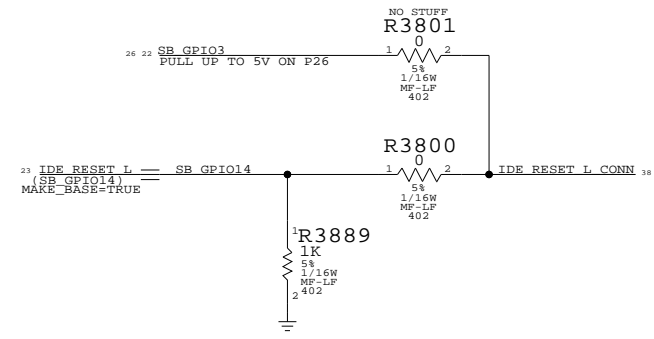
SYNC_MASTER=M51_HENRY SYNC_DATE=08/04/2006

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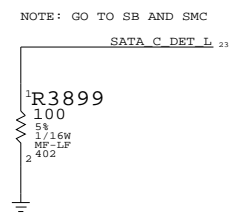
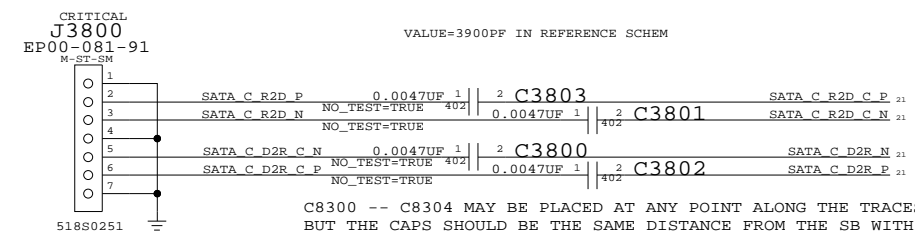
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7039	M
SCALE	SHT	34 OF 97	
NONE			

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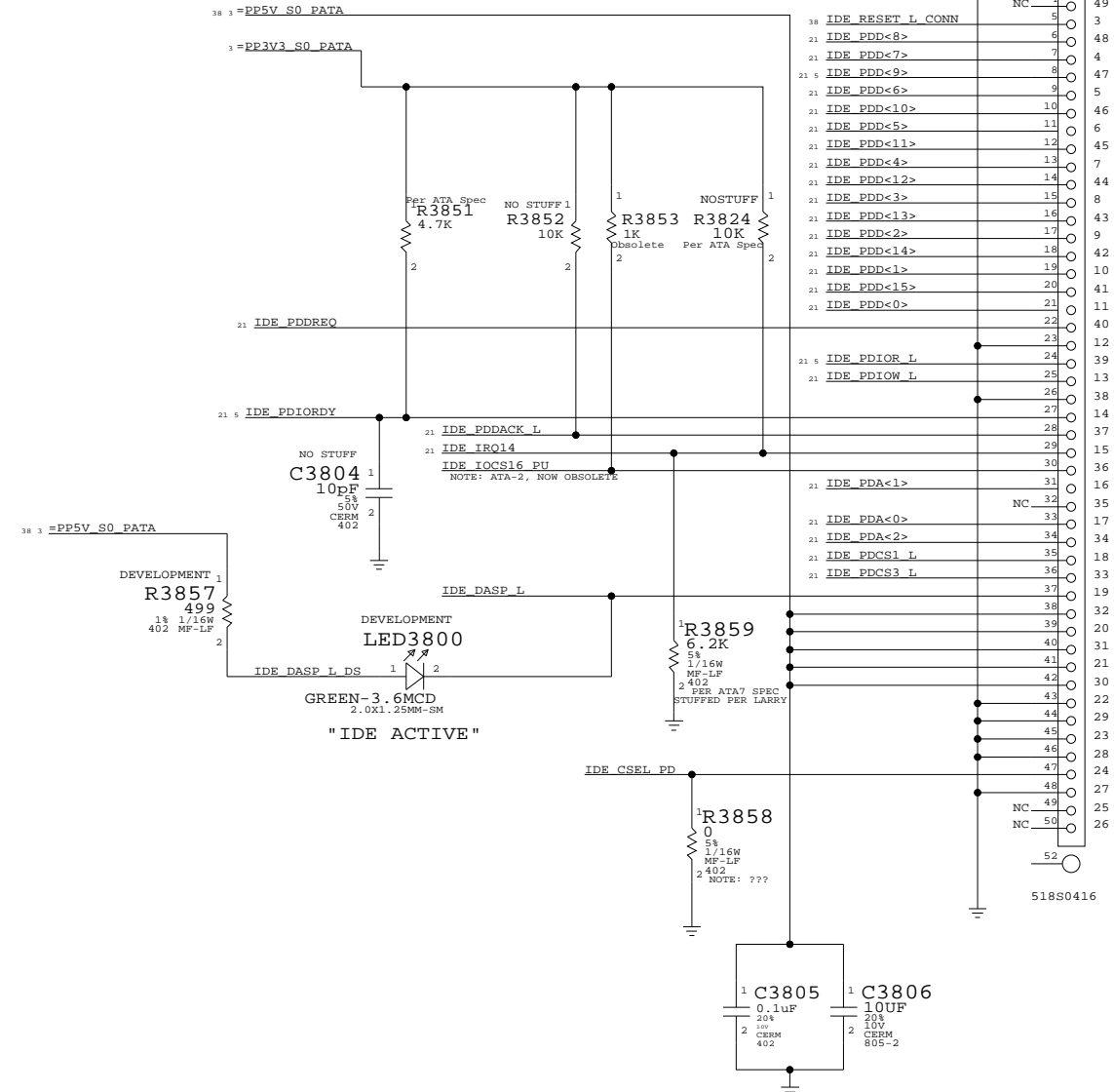
PATA (ODD) CONNECTOR



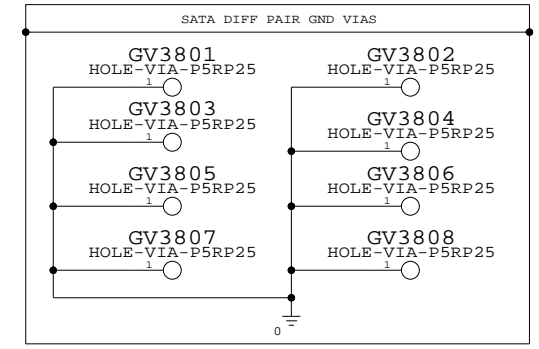
SATA CONNECTOR



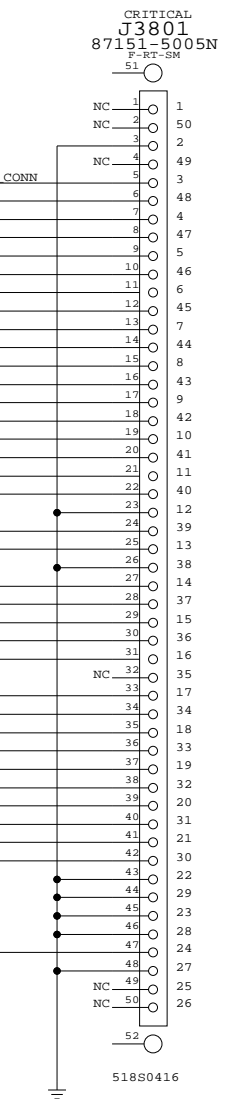
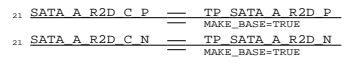
NOTE: GO TO SB AND SMC



PLACE C3805-06 CLOSE TO J3801 FOR PP5V_S0_PATA. APPLY A WIDE TRACE SHAPE FROM J3801 TO C3805-06. MIN NECK & MIN LINE WIDTH ARE CONTROLLED BY PP5V_S0 1MM / 0.6MM.



SATA PORT 0 IS NOT USED



Disk Connectors

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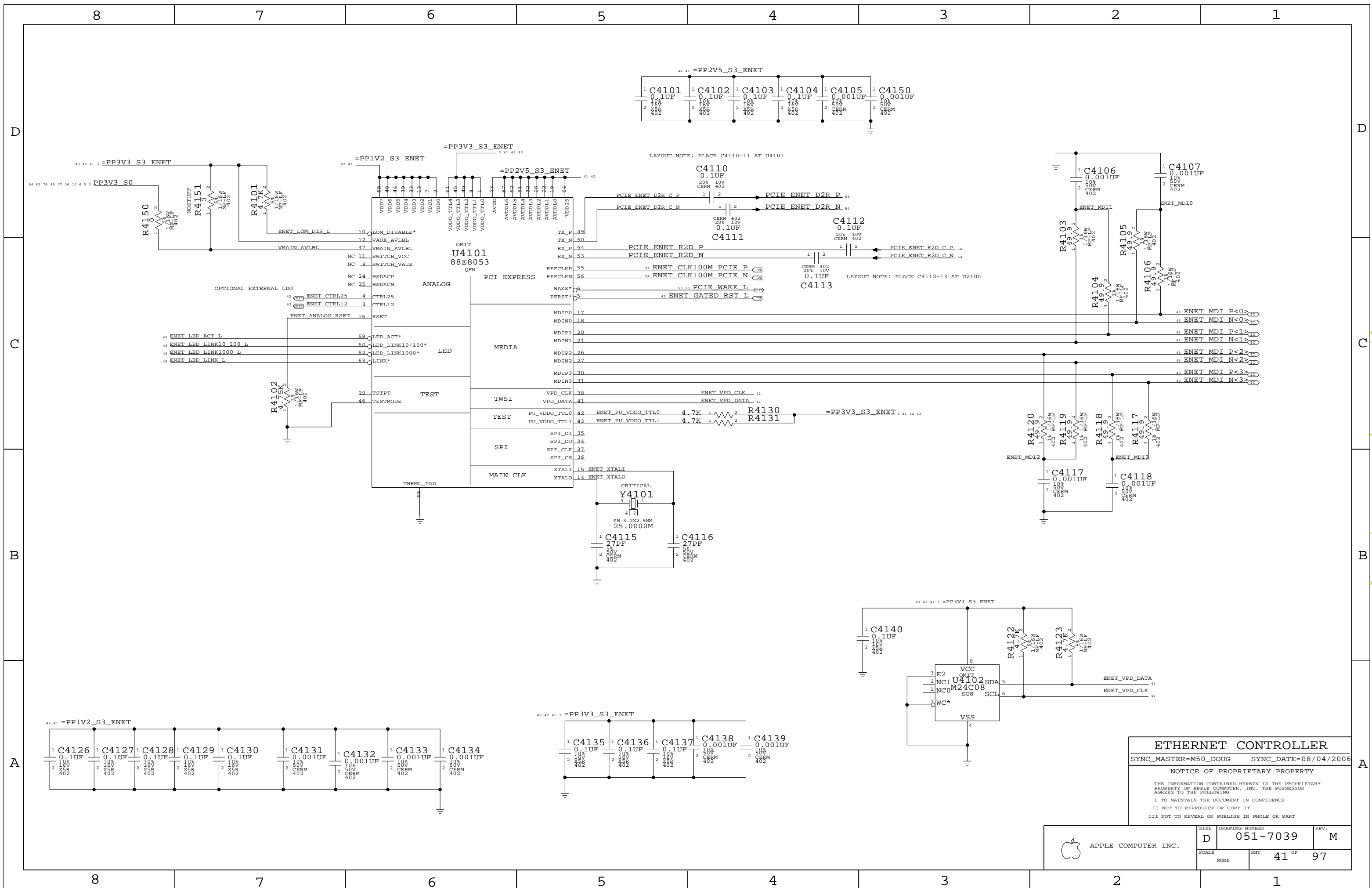
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	M
SCALE	SHT	38 OF 97
NONE		

D
C
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D
C
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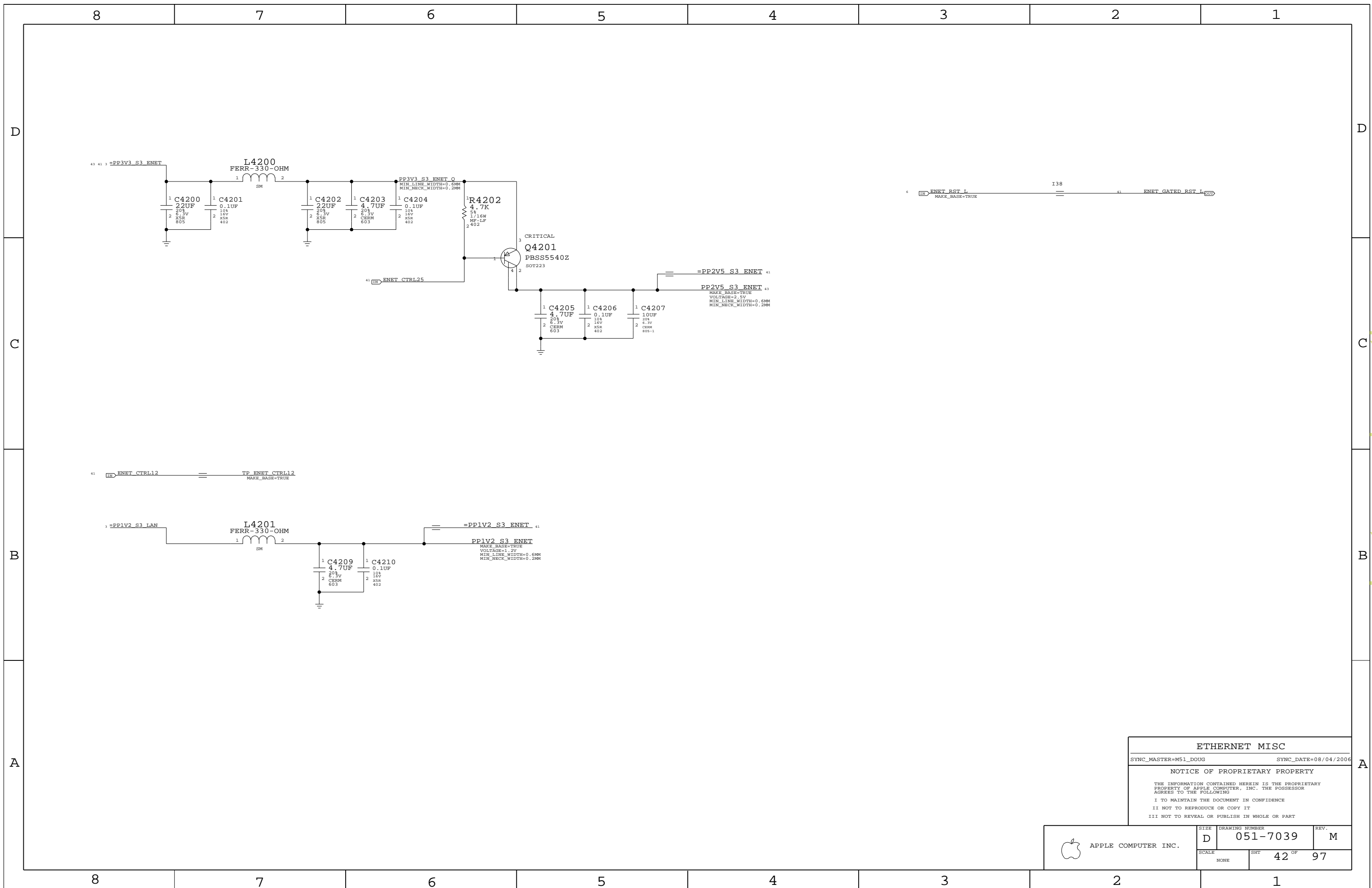
ETHERNET CONTROLLER

SYNC_MASTER=M50_DOUG SYNC_DATE=08/04/2006

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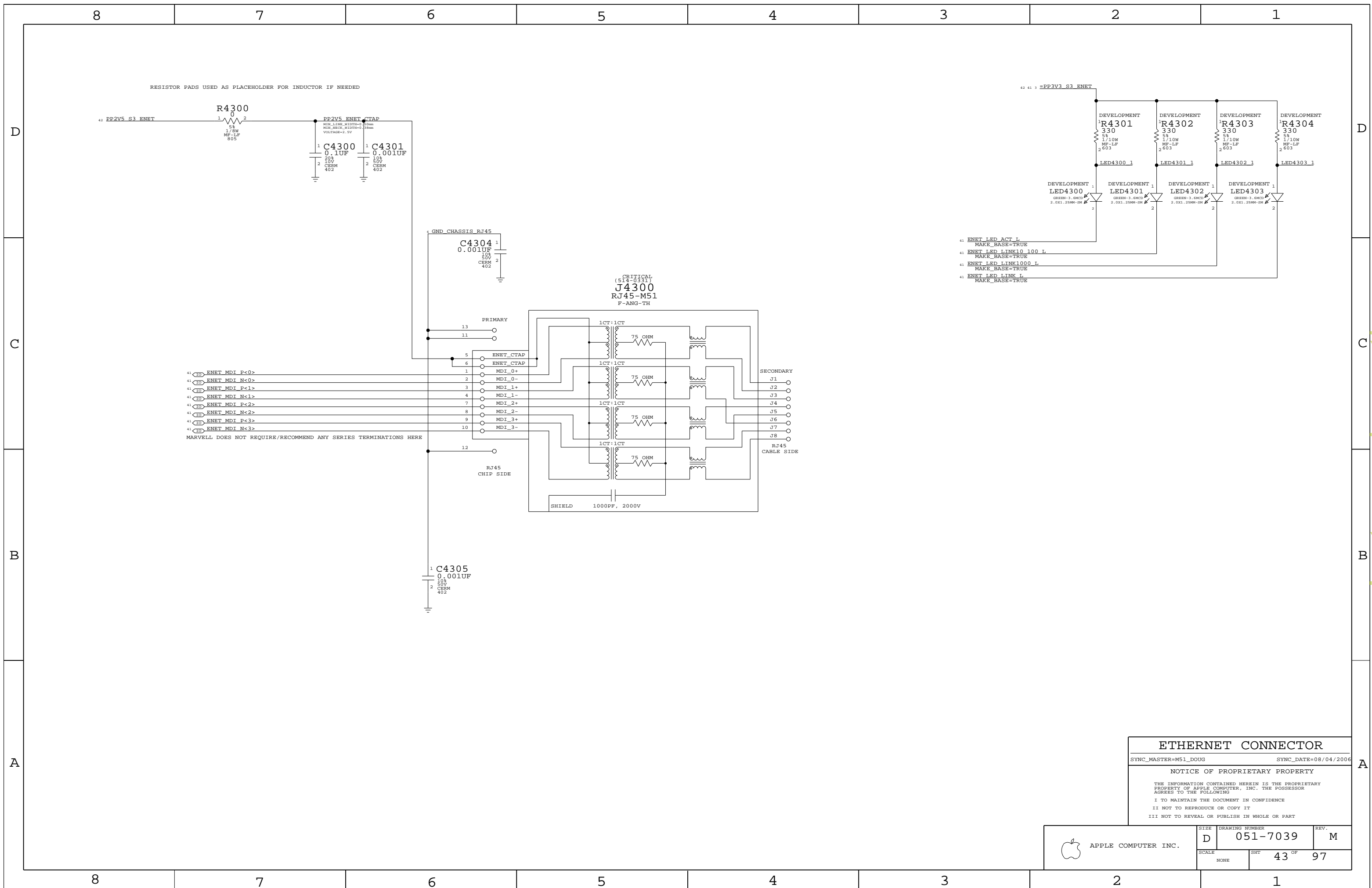
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7039	M
SCALE	SHT	41 OF 97	
NONE			



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ETHERNET MISC
 SYNC_MASTER=M51_DOUG SYNC_DATE=08/04/2006
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7039	M
SCALE	SHT	42 OF 97	
NONE			



ETHERNET CONNECTOR

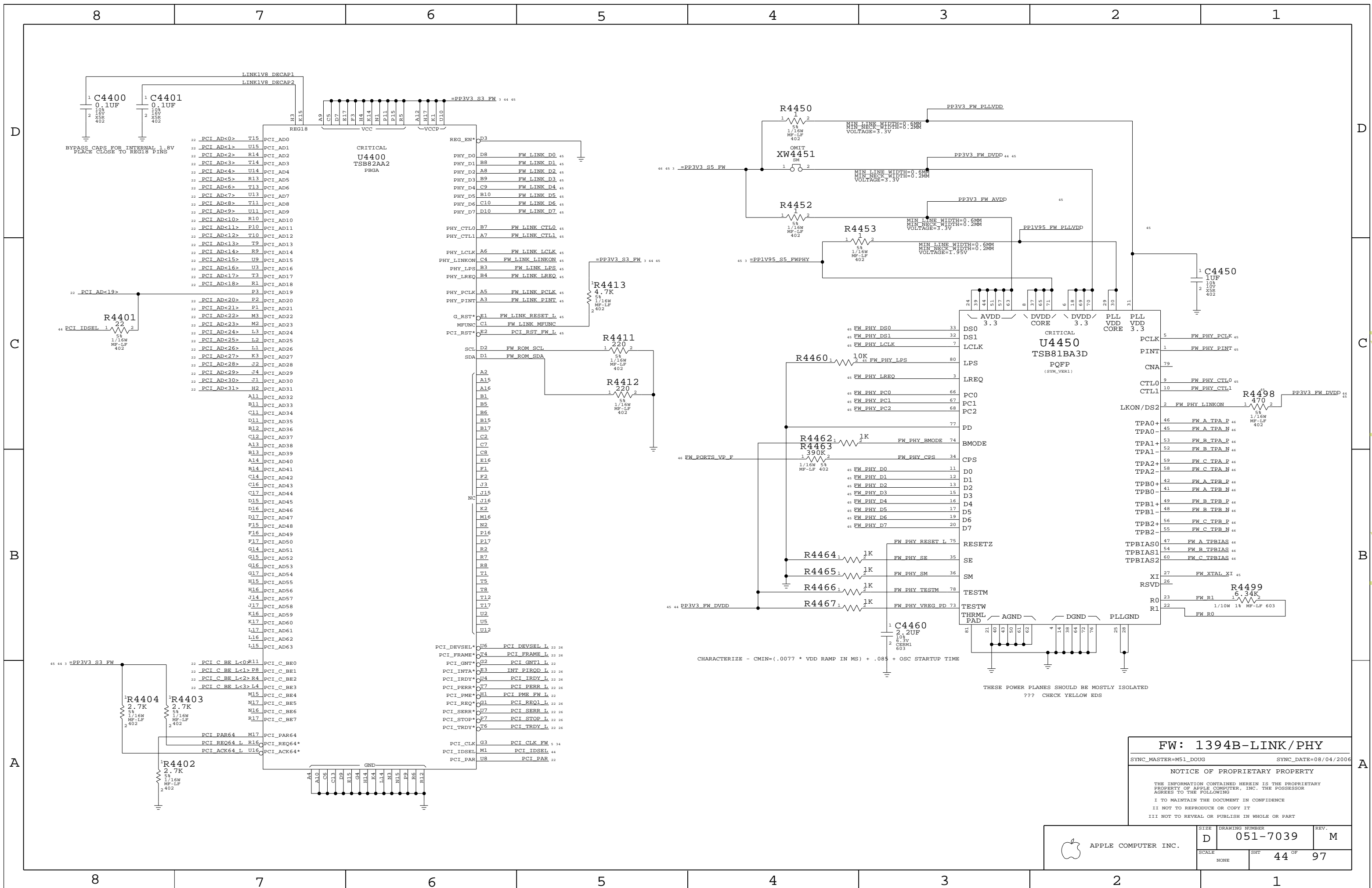
SYNC_MASTER=M51_DOUG SYNC_DATE=08/04/2006

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7039	REV. M
	SCALE NONE	SHT 43 OF 97	

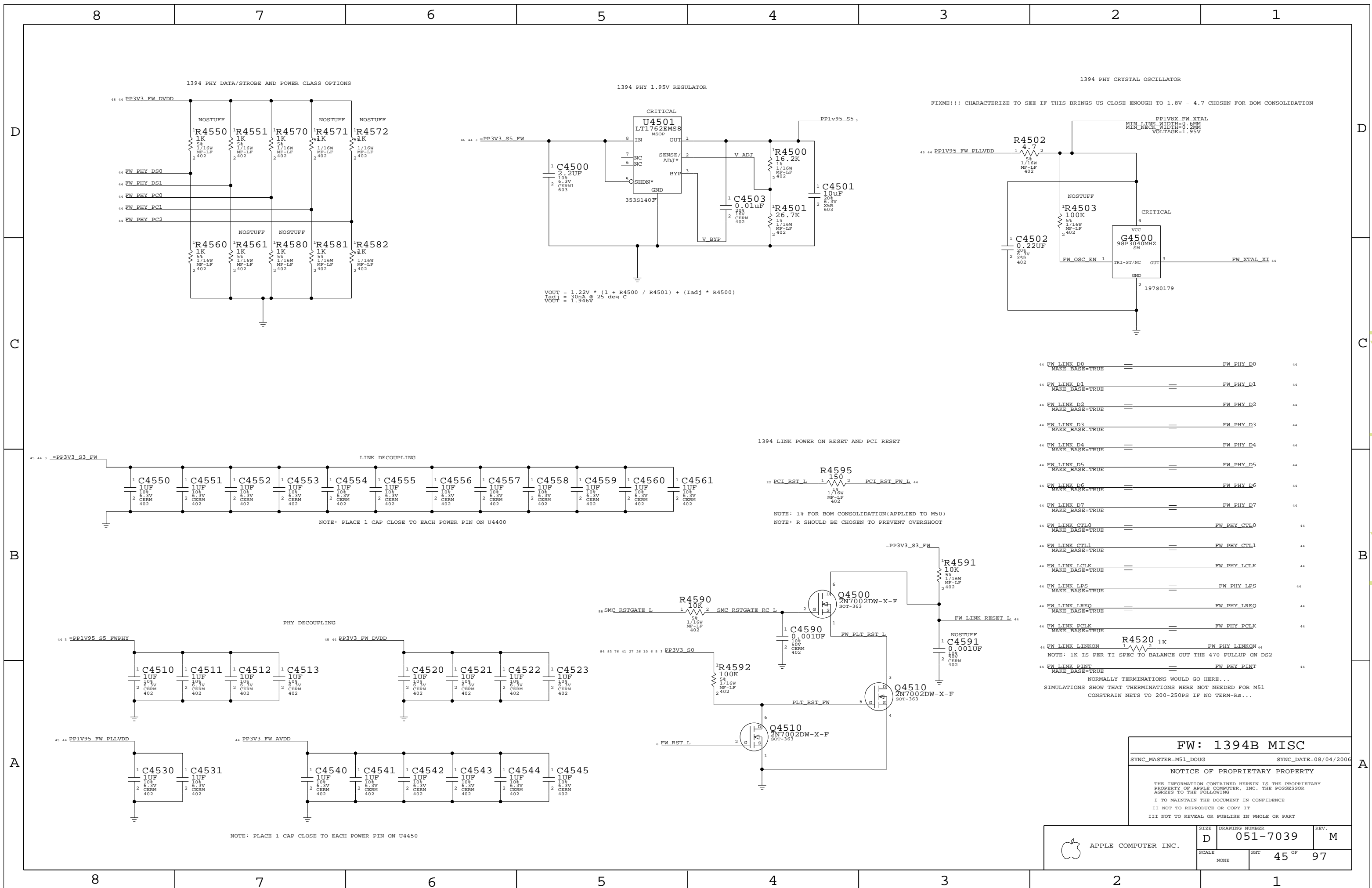


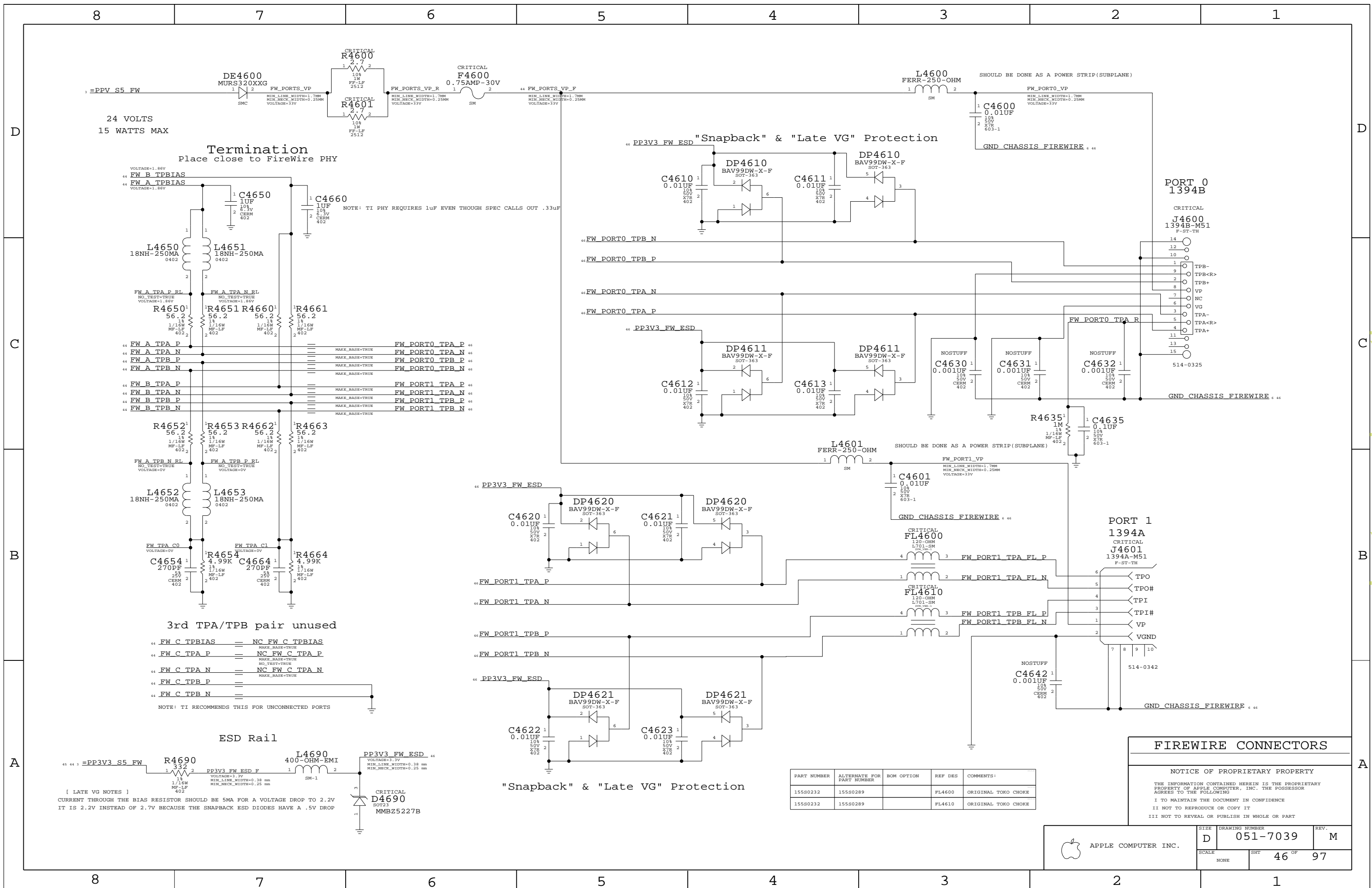
FW: 1394B-LINK/PHY
 SYNC_MASTER=M51_D0UG SYNC_DATE=08/04/2006

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	D	051-7039	M
SCALE	SHT	44 OF 97	
NONE			

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FIREWIRE CONNECTORS

NOTICE OF PROPRIETARY PROPERTY

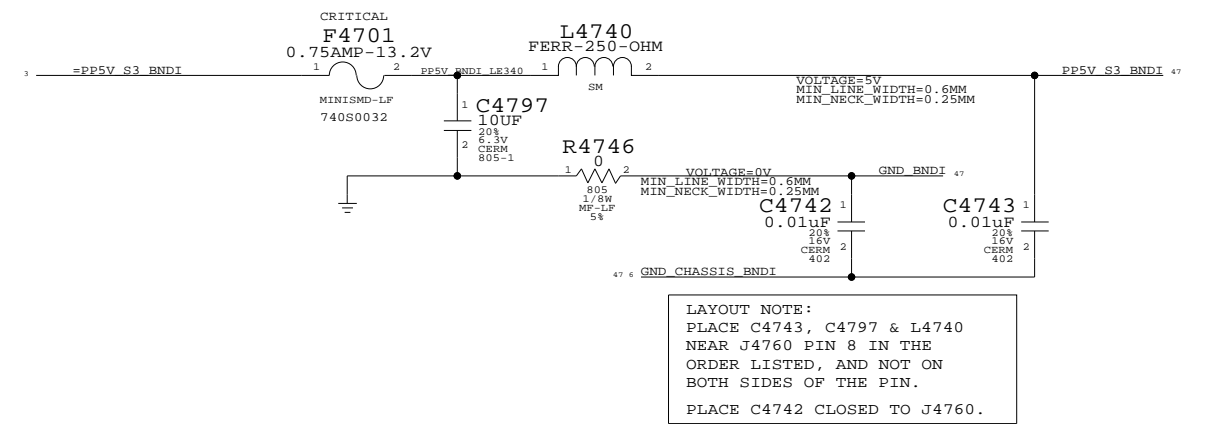
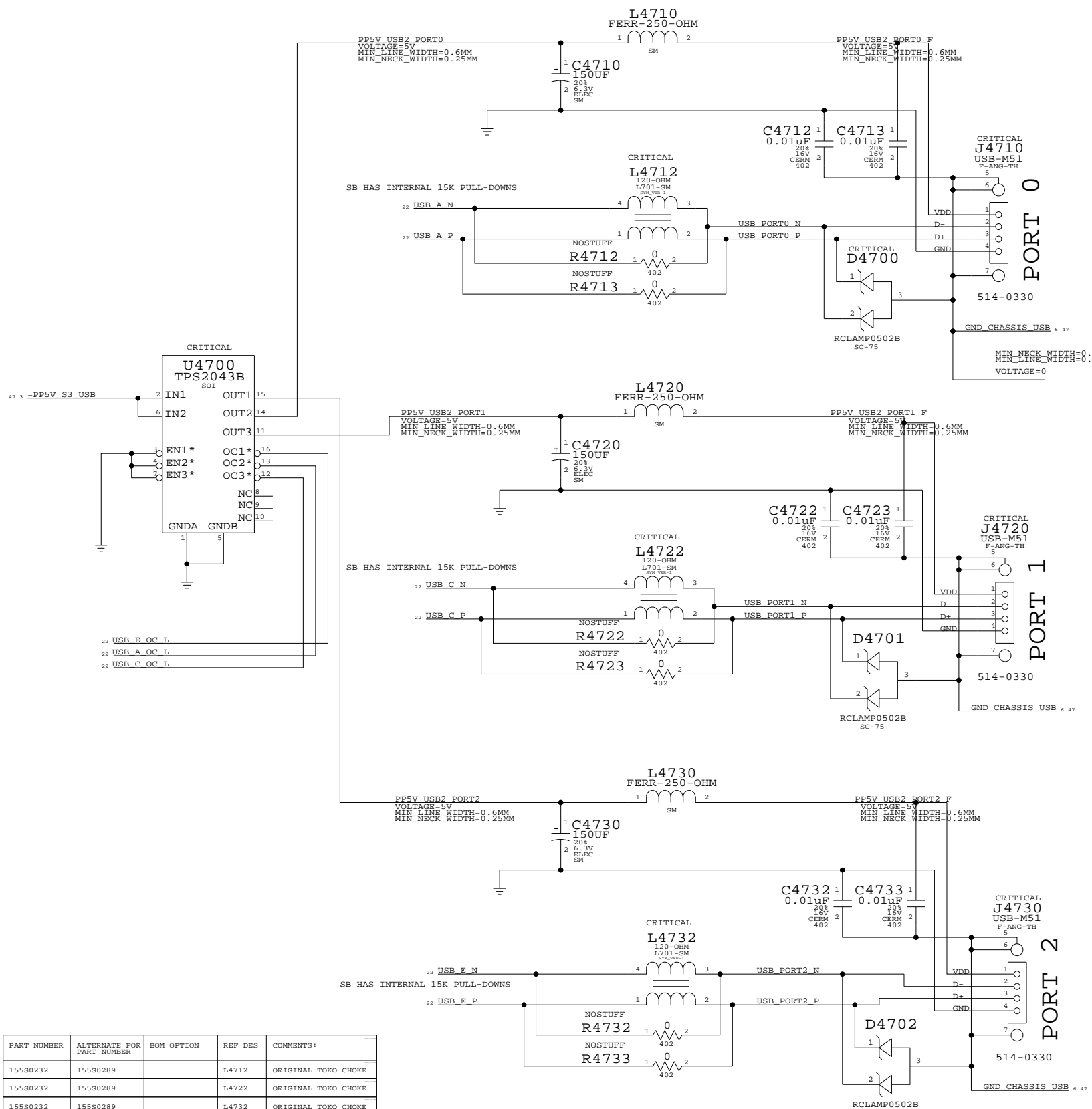
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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
15580232	15580289		FL4600	ORIGINAL TOKO CHOKE
15580232	15580289		FL4610	ORIGINAL TOKO CHOKE

APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7039	REV. M
	SCALE NONE	SHEET 46 OF 97	

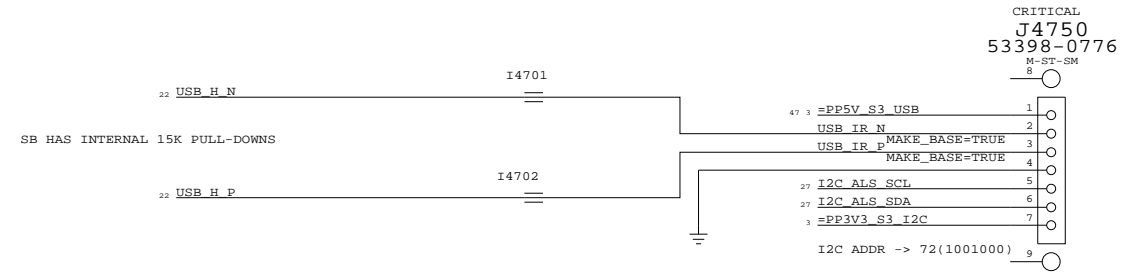
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External USB Ports

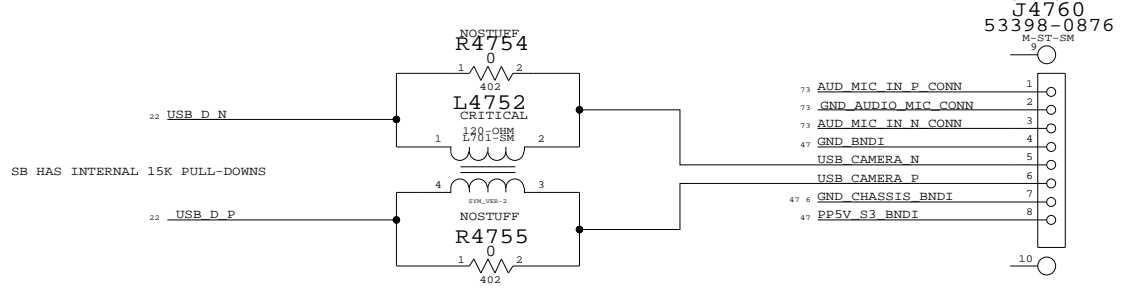


LAYOUT NOTE:
PLACE C4743, C4797 & L4740
NEAR J4760 PIN 8 IN THE
ORDER LISTED, AND NOT ON
BOTH SIDES OF THE PIN.
PLACE C4742 CLOSED TO J4760.

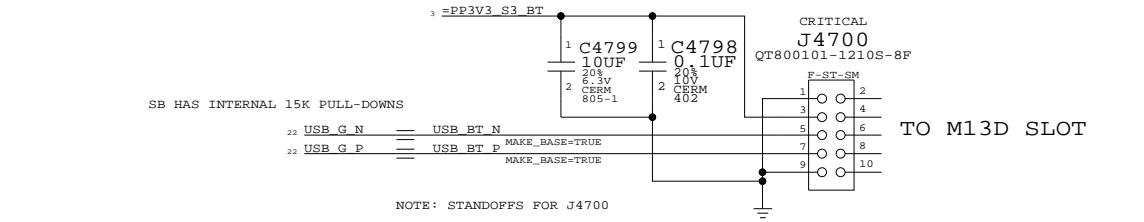
IR RECEIVER & ALS



CAMERA & MIC

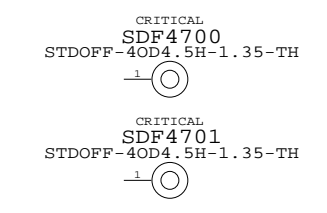


BLUETOOTH



TO M13D SLOT

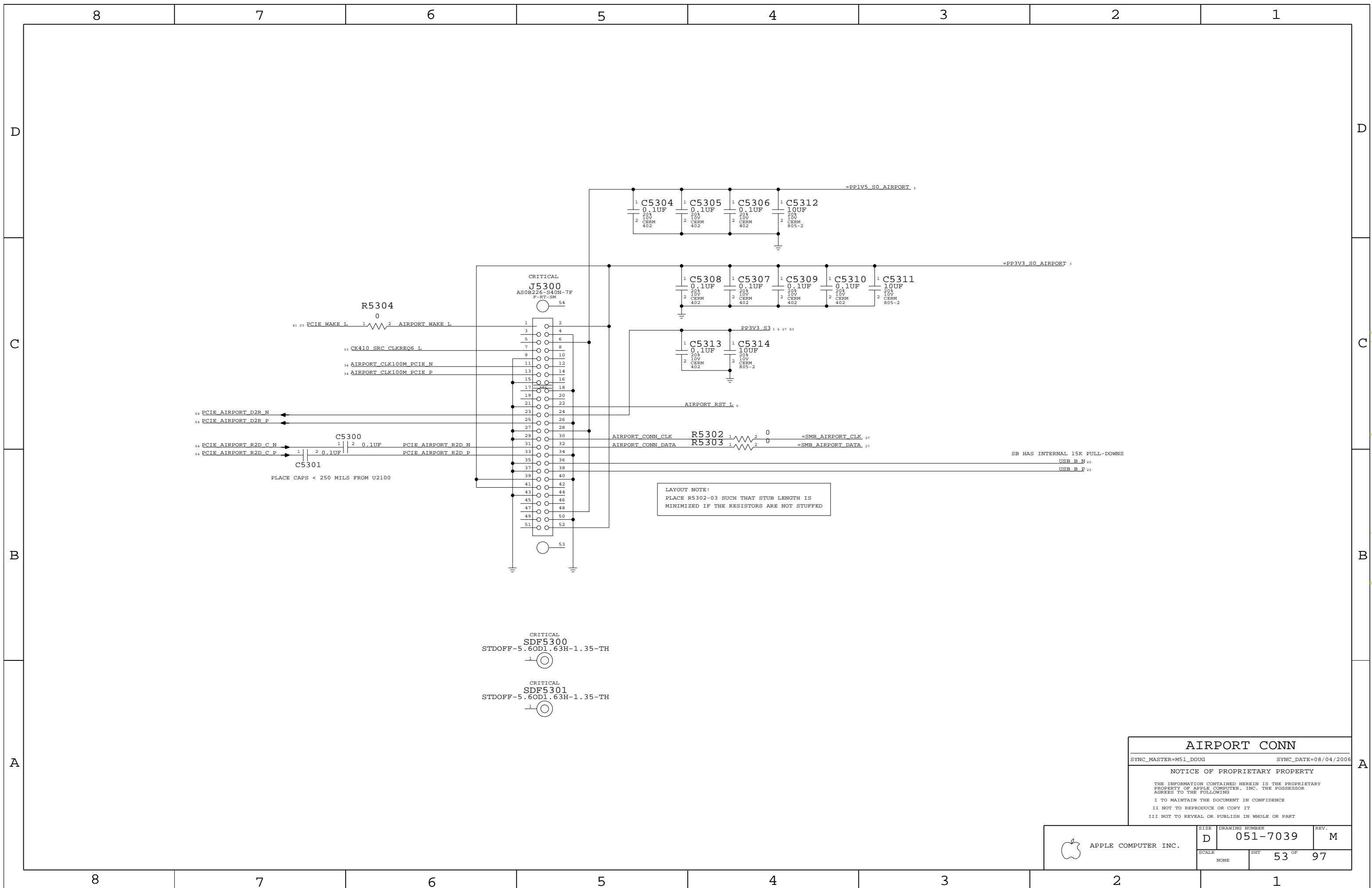
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0232	155S0289		L4712	ORIGINAL TOKO CHOKE
155S0232	155S0289		L4722	ORIGINAL TOKO CHOKE
155S0232	155S0289		L4732	ORIGINAL TOKO CHOKE
155S0232	155S0289		L4752	ORIGINAL TOKO CHOKE



USB Device Interfaces
 SYNC_MASTER=M51_D0UG SYNC_DATE=08/04/2006
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	D	051-7039	M
SCALE	SHT	47 OF	97
NONE			

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LAYOUT NOTE:
 PLACE R5302-03 SUCH THAT STUB LENGTH IS
 MINIMIZED IF THE RESISTORS ARE NOT STUFFED

CRITICAL
 SDF5300
 STDOFF-5.60D1.63H-1.35-TH

CRITICAL
 SDF5301
 STDOFF-5.60D1.63H-1.35-TH

PLACE CAPS < 250 MILS FROM U2100

SB HAS INTERNAL 15K PULL-DOWNS
 USB_B_N 22
 USB_B_P 22

AIRPORT CONN	
SYNC_MASTER=M51_DOUG	SYNC_DATE=08/04/2006
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	D	051-7039	M
SCALE	SHT	REV.	
NONE	53 OF	97	

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D

D

C

C

B

B

A

A

PCI-E X1 PORT "A" = ETHERNET (YUKON)

22 PCIE_A_R2D_C_N == PCIE_ENET_R2D_C_N 41
MAKE_BASE=TRUE

22 PCIE_A_R2D_C_P == PCIE_ENET_R2D_C_P 41
MAKE_BASE=TRUE

22 PCIE_A_D2R_N == PCIE_ENET_D2R_N 41
MAKE_BASE=TRUE

22 PCIE_A_D2R_P == PCIE_ENET_D2R_P 41
MAKE_BASE=TRUE

PCI-E X1 PORT "B" = MINI CARD (AIRPORT)

22 PCIE_B_R2D_C_N == PCIE_AIRPORT_R2D_C_N 43
MAKE_BASE=TRUE

22 PCIE_B_R2D_C_P == PCIE_AIRPORT_R2D_C_P 43
MAKE_BASE=TRUE

22 PCIE_B_D2R_N == PCIE_AIRPORT_D2R_N 43
MAKE_BASE=TRUE

22 PCIE_B_D2R_P == PCIE_AIRPORT_D2R_P 43
MAKE_BASE=TRUE

PCI-E X1 PORTS C, D, E, F = UNUSED

22 PCIE_C_R2D_C_N == TP_PCIE_C_R2D_C_N
MAKE_BASE=TRUE

22 PCIE_C_R2D_C_P == TP_PCIE_C_R2D_C_P
MAKE_BASE=TRUE

22 PCIE_C_D2R_N == TP_PCIE_C_D2R_N
MAKE_BASE=TRUE

22 PCIE_C_D2R_P == TP_PCIE_C_D2R_P
MAKE_BASE=TRUE

22 PCIE_D_R2D_C_N == TP_PCIE_D_R2D_C_N
MAKE_BASE=TRUE

22 PCIE_D_R2D_C_P == TP_PCIE_D_R2D_C_P
MAKE_BASE=TRUE

22 PCIE_D_D2R_N == TP_PCIE_D_D2R_N
MAKE_BASE=TRUE

22 PCIE_D_D2R_P == TP_PCIE_D_D2R_P
MAKE_BASE=TRUE

22 PCIE_E_R2D_C_N == TP_PCIE_E_R2D_C_N
MAKE_BASE=TRUE

22 PCIE_E_R2D_C_P == TP_PCIE_E_R2D_C_P
MAKE_BASE=TRUE

22 PCIE_E_D2R_N == TP_PCIE_E_D2R_N
MAKE_BASE=TRUE

22 PCIE_E_D2R_P == TP_PCIE_E_D2R_P
MAKE_BASE=TRUE

22 PCIE_F_R2D_C_N == TP_PCIE_F_R2D_C_N
MAKE_BASE=TRUE

22 PCIE_F_R2D_C_P == TP_PCIE_F_R2D_C_P
MAKE_BASE=TRUE

22 PCIE_F_D2R_N == TP_PCIE_F_D2R_N
MAKE_BASE=TRUE

22 PCIE_F_D2R_P == TP_PCIE_F_D2R_P
MAKE_BASE=TRUE

PCI-E CONNECTIONS

SYNC_MASTER=M51_DOUG SYNC_DATE=08/04/2006

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	M
SCALE	SHT	54 OF 97
NONE		

8

7

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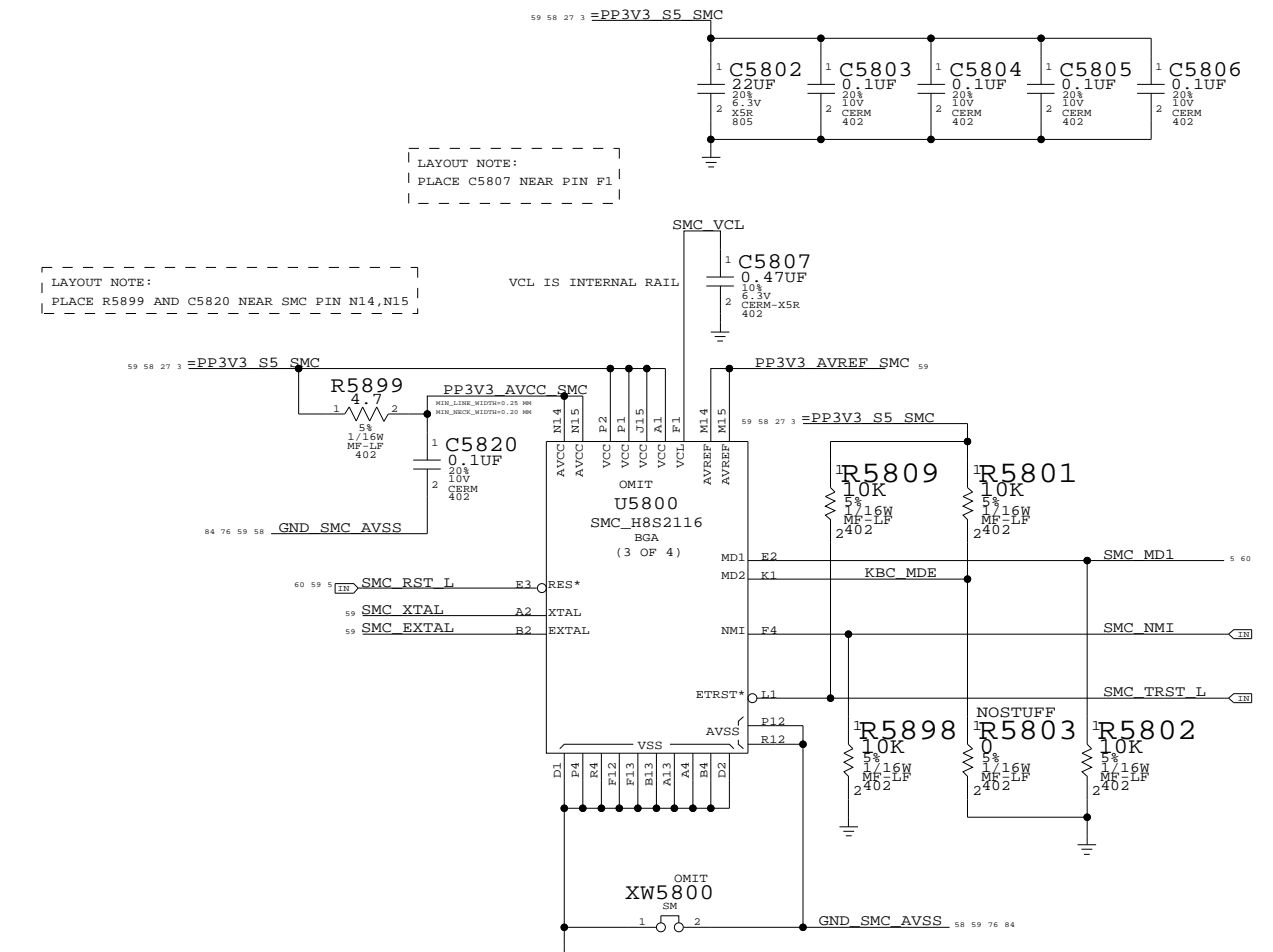
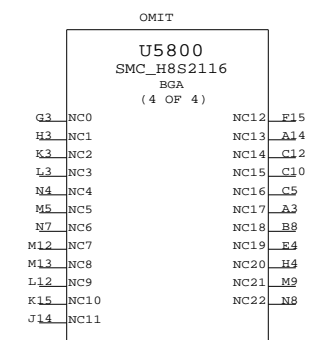
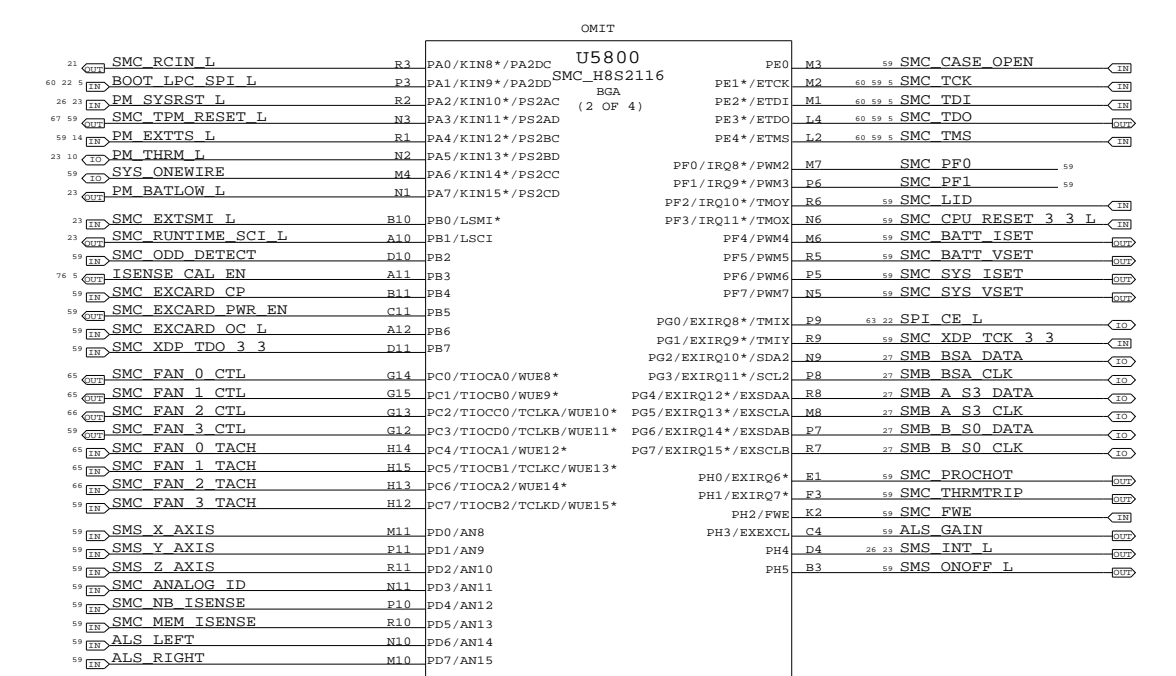
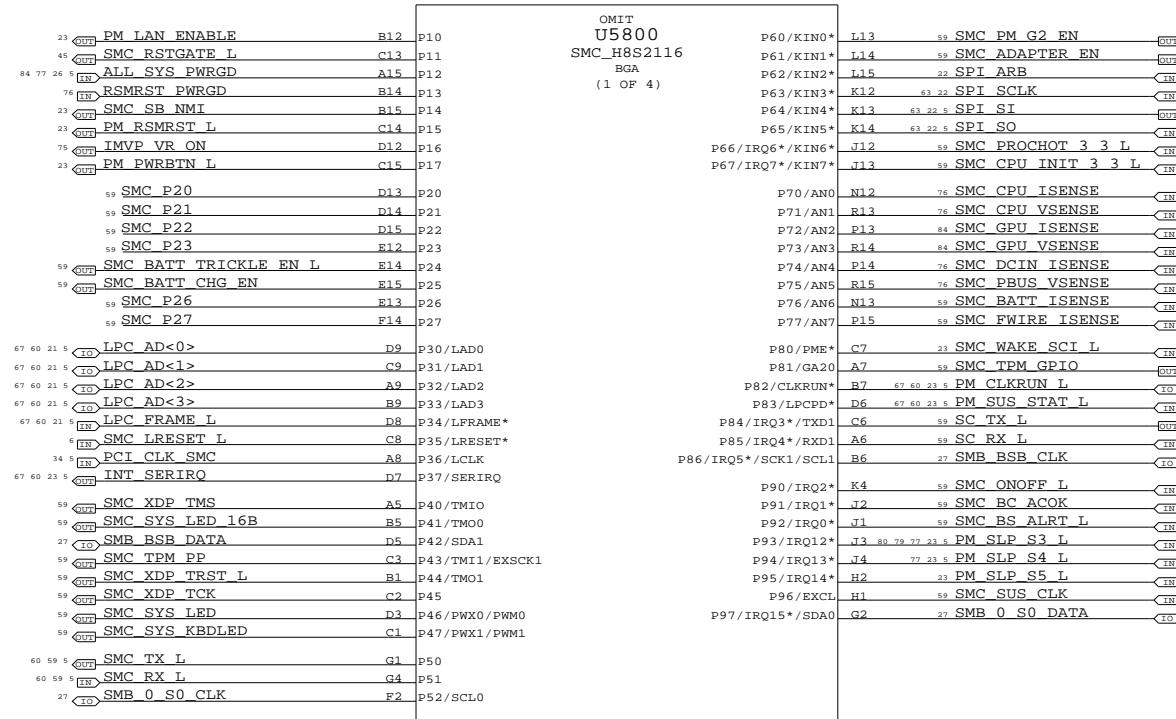
3

2

1

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UNUSED PINS HAVE THE FORMAT SMC_XXX WHERE XXX IS THE PORT NUMBER. THEY ARE SET BY SOFTWARE TO BE DRIVEN OUTPUTS ALWAYS SO THEY CAN BE LEFT NO-CONNECTED.



SMC

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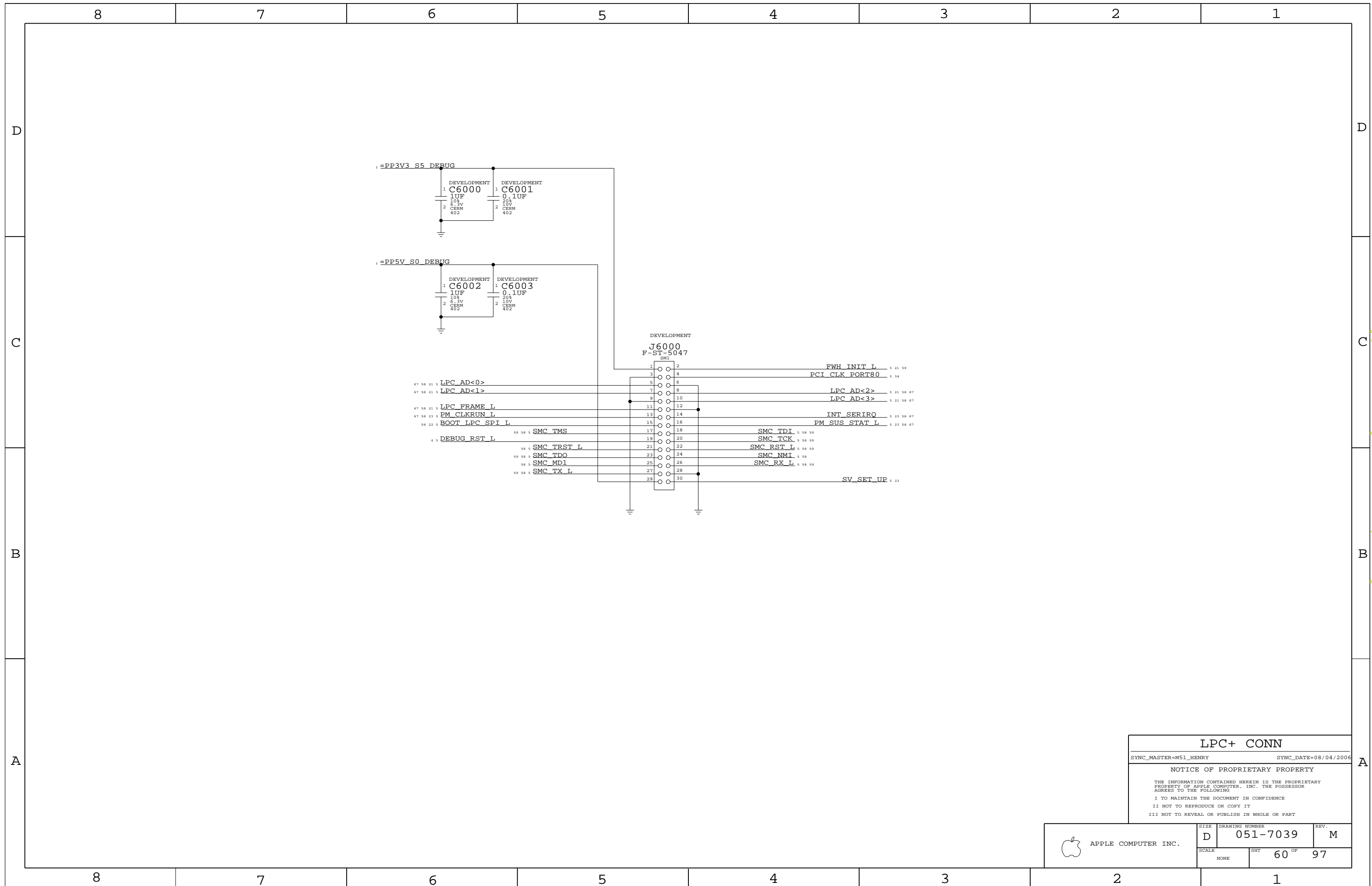
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7039	M
SCALE	SHT	58 OF	97
NONE			

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LPC+ CONN

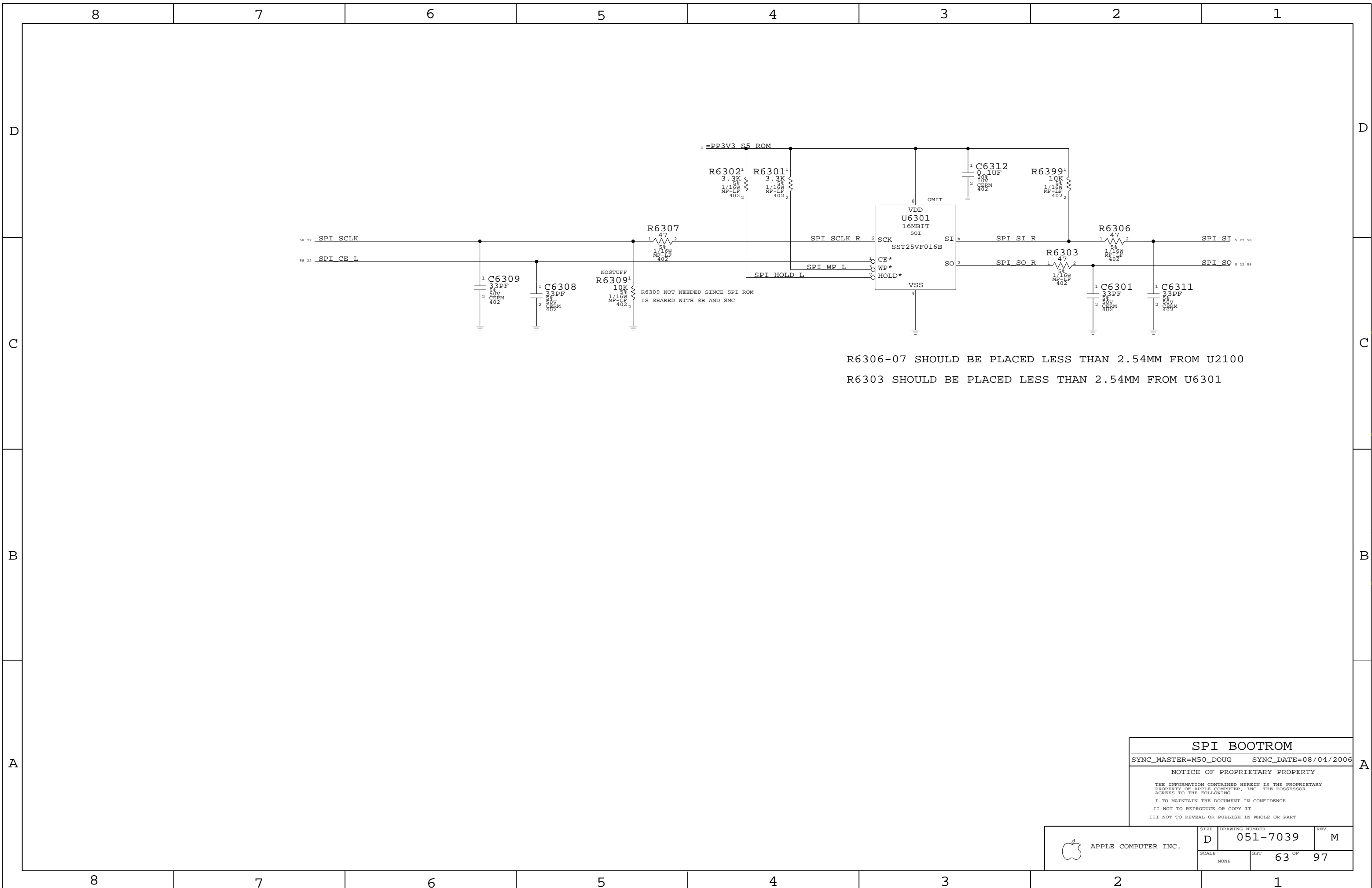
SYNC_MASTER=M51_HENRY SYNC_DATE=08/04/2006

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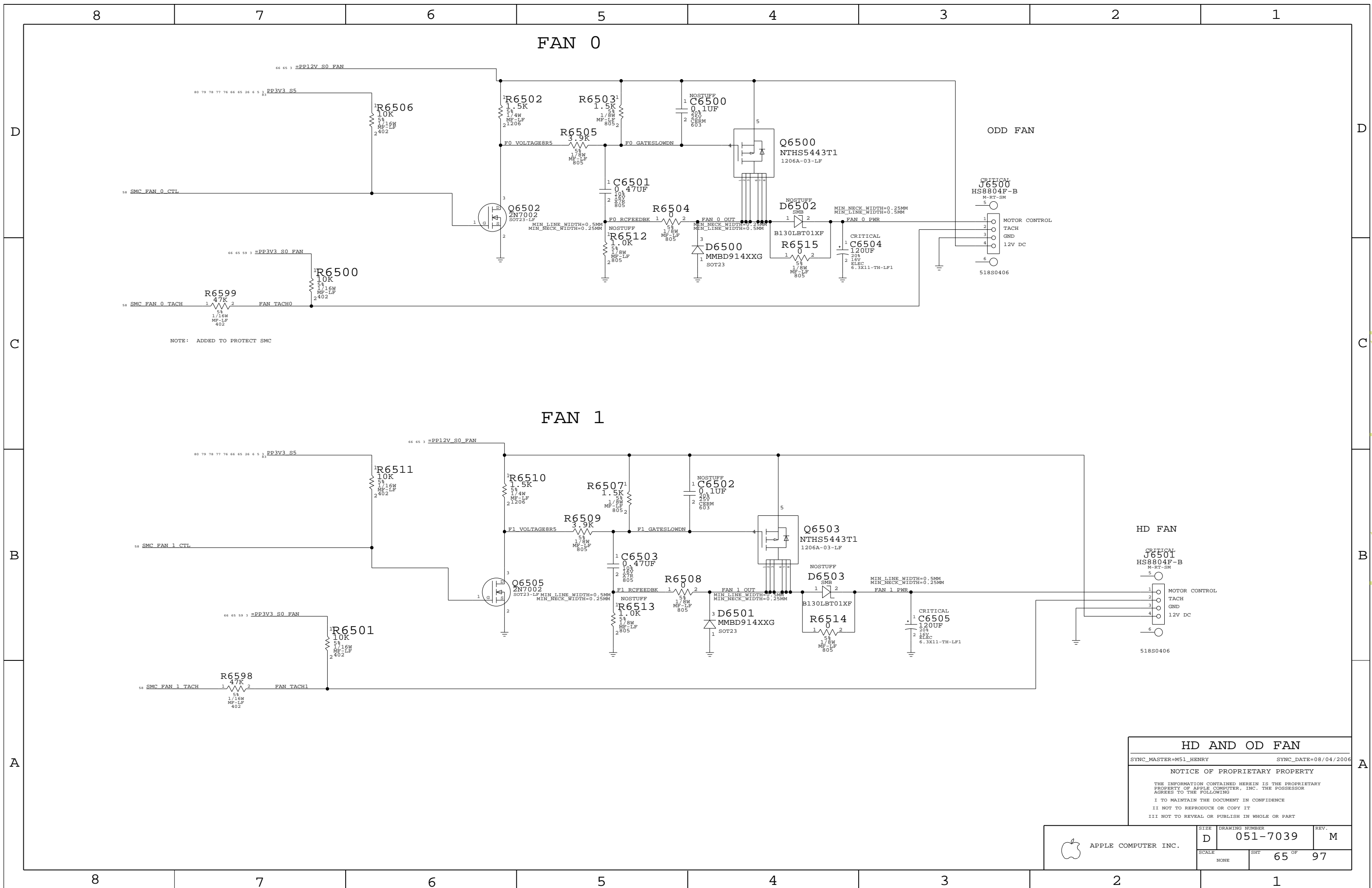
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7039	REV. M
	SCALE NONE	SHT 60 OF 97	



R6306-07 SHOULD BE PLACED LESS THAN 2.54MM FROM U2100
 R6303 SHOULD BE PLACED LESS THAN 2.54MM FROM U6301

SPI BOOTROM
 SYNC_MASTER=M50_DOUG SYNC_DATE=08/04/2006
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7039	M
SCALE	SHT	63 OF 97	
NONE			

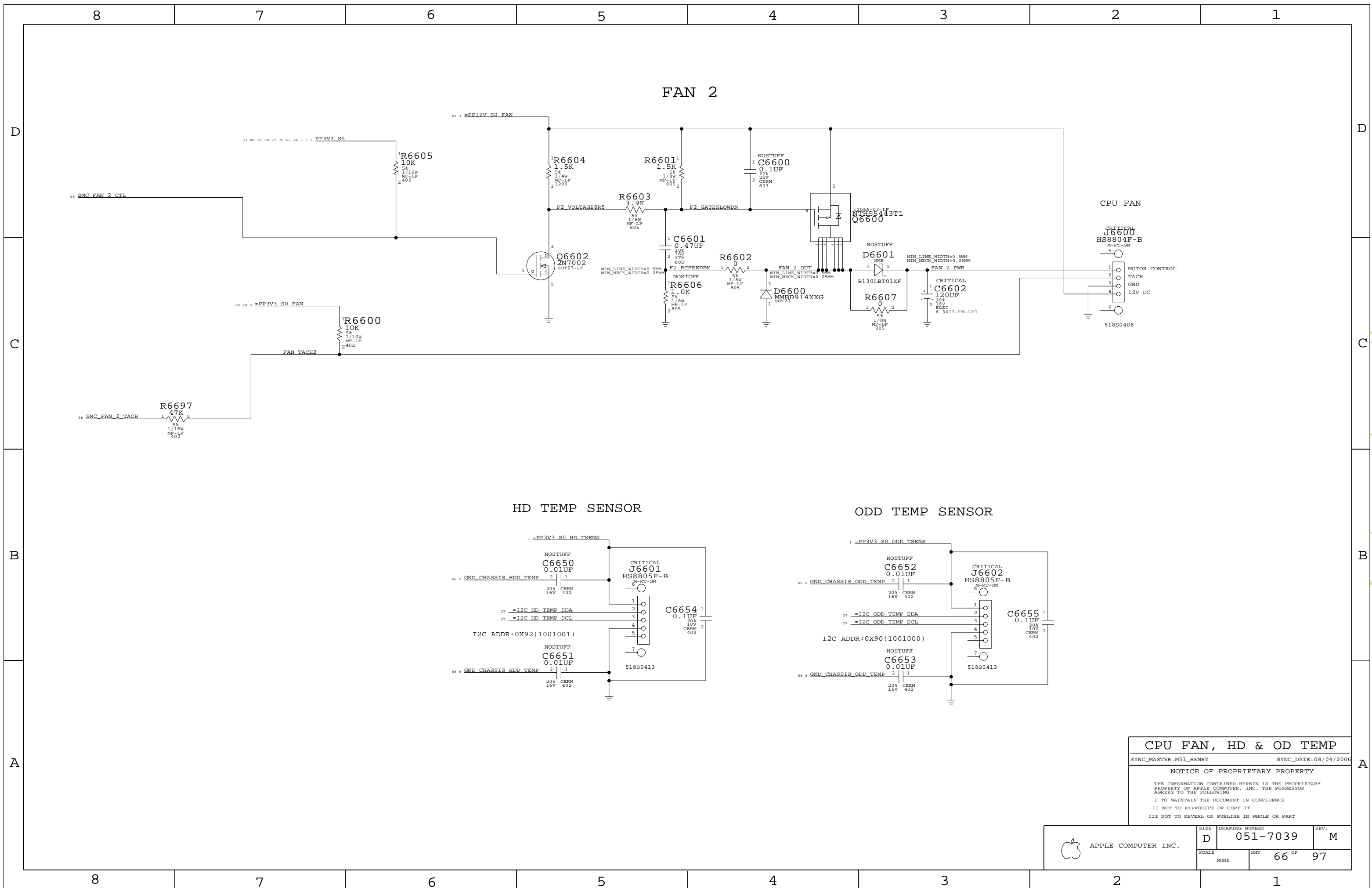


NOTE: ADDED TO PROTECT SMC

HD AND OD FAN
 SYNC_MASTER=M51_HENRY SYNC_DATE=08/04/2006
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	D	051-7039	M
SCALE	SHT	65 OF	97
NONE			

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CPU FAN, HD & OD TEMP

SYNC_MASTER=M51_HENRY SYNC_DATE=08/04/2006

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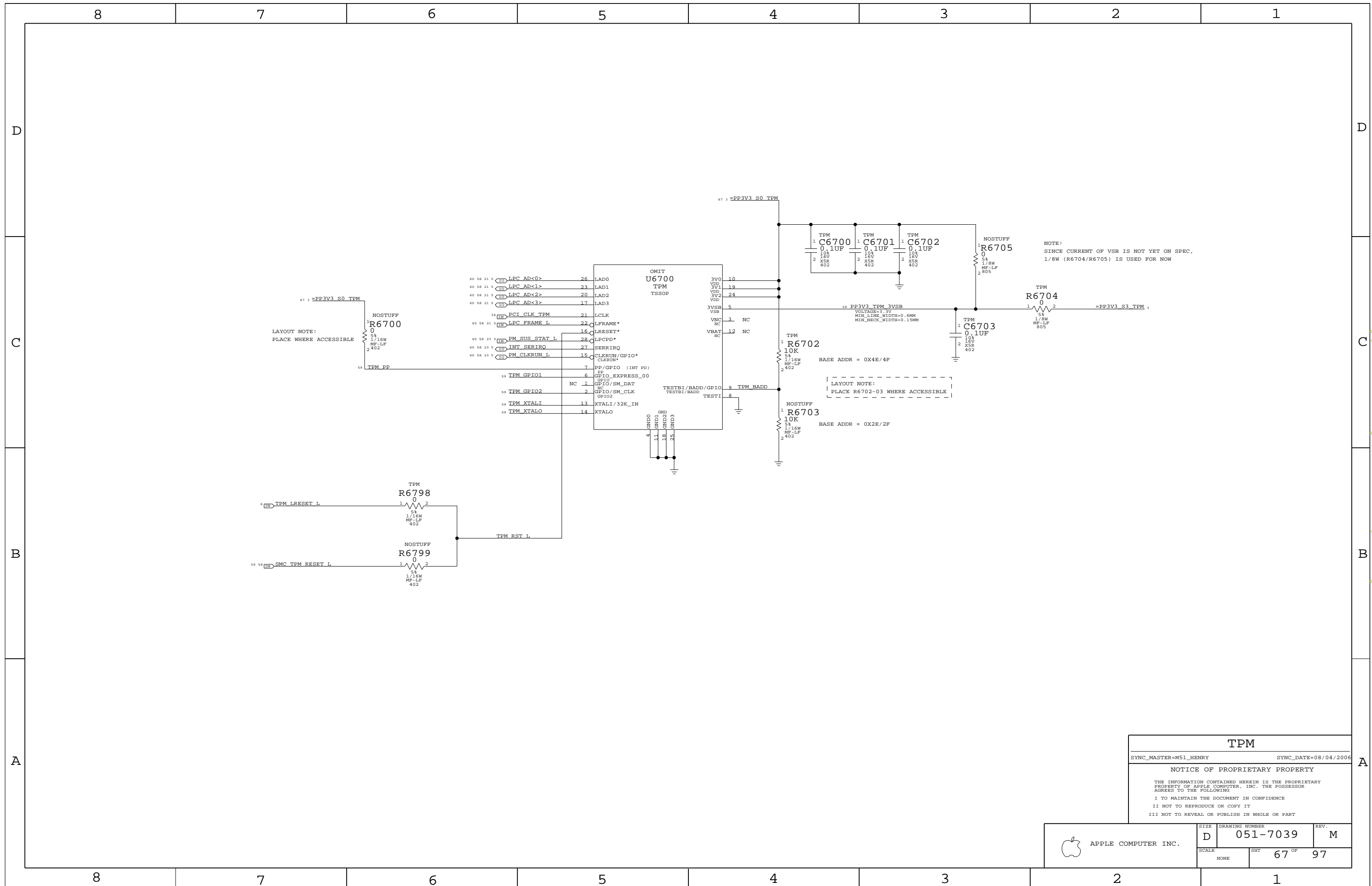
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7039	M
SCALE	SHT	66 OF	97
NONE			



LAYOUT NOTE:
PLACE WHERE ACCESSIBLE

LAYOUT NOTE:
PLACE R6702-03 WHERE ACCESSIBLE

NOTE:
SINCE CURRENT OF VSB IS NOT YET ON SPEC,
1/8W (R6704/R6705) IS USED FOR NOW

TPM

SYNC_MASTER=M51_HENRY SYNC_DATE=08/04/2006

NOTICE OF PROPRIETARY PROPERTY

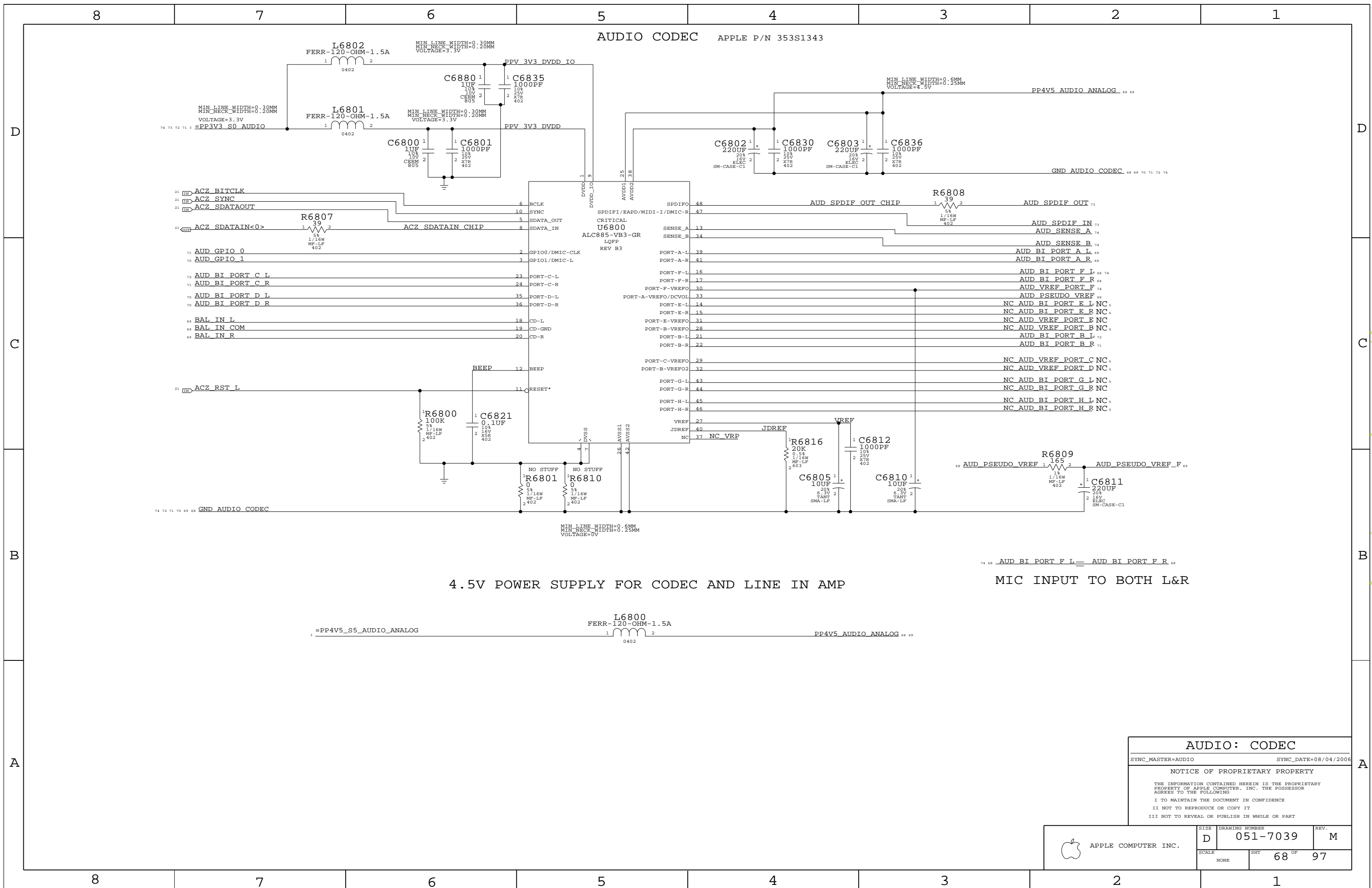
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	D	051-7039	M
SCALE	SHT	67 OF 97	
NONE			



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AUDIO: CODEC

SYNC_MASTER=AUDIO SYNC_DATE=08/04/2006

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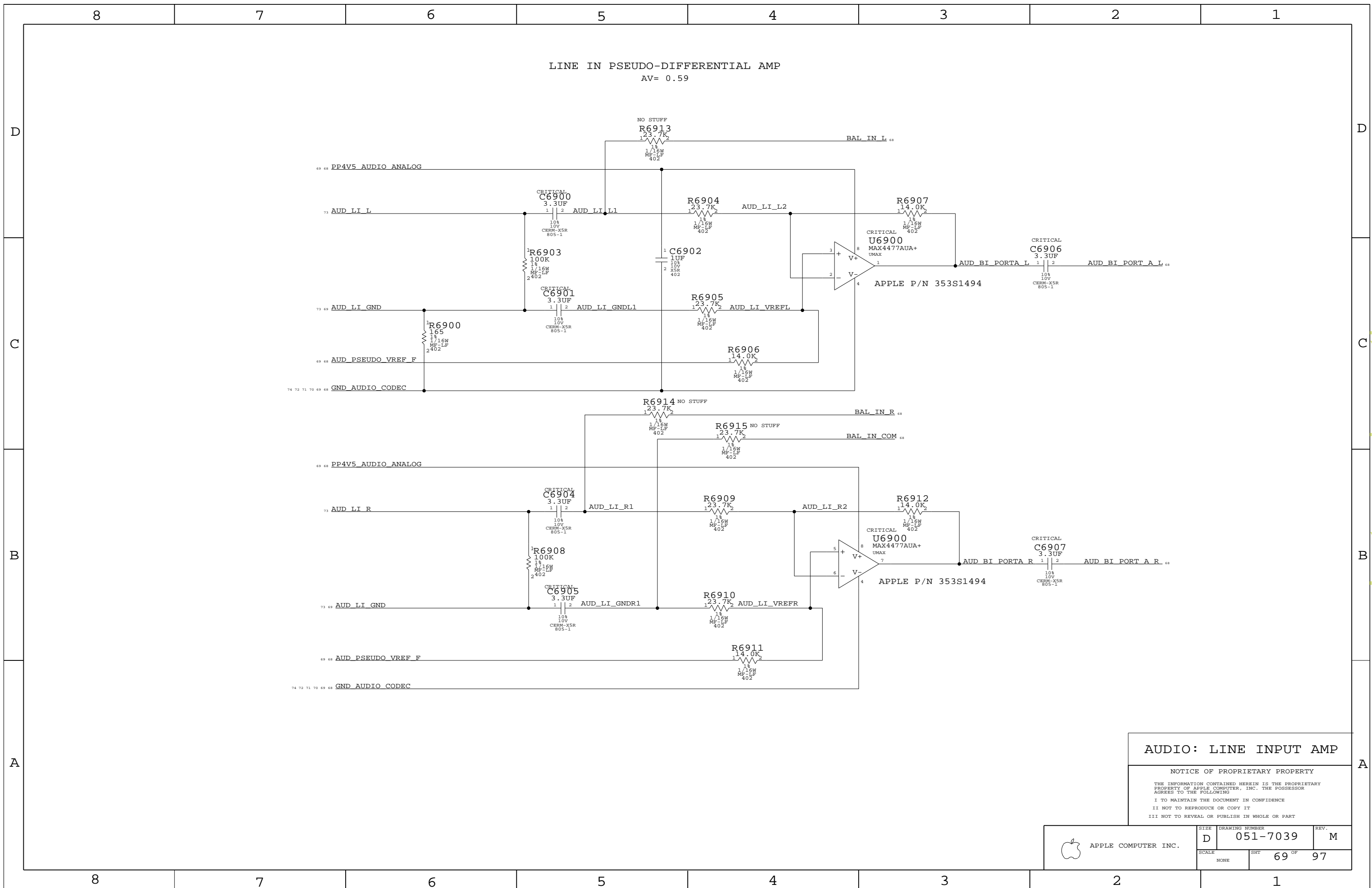
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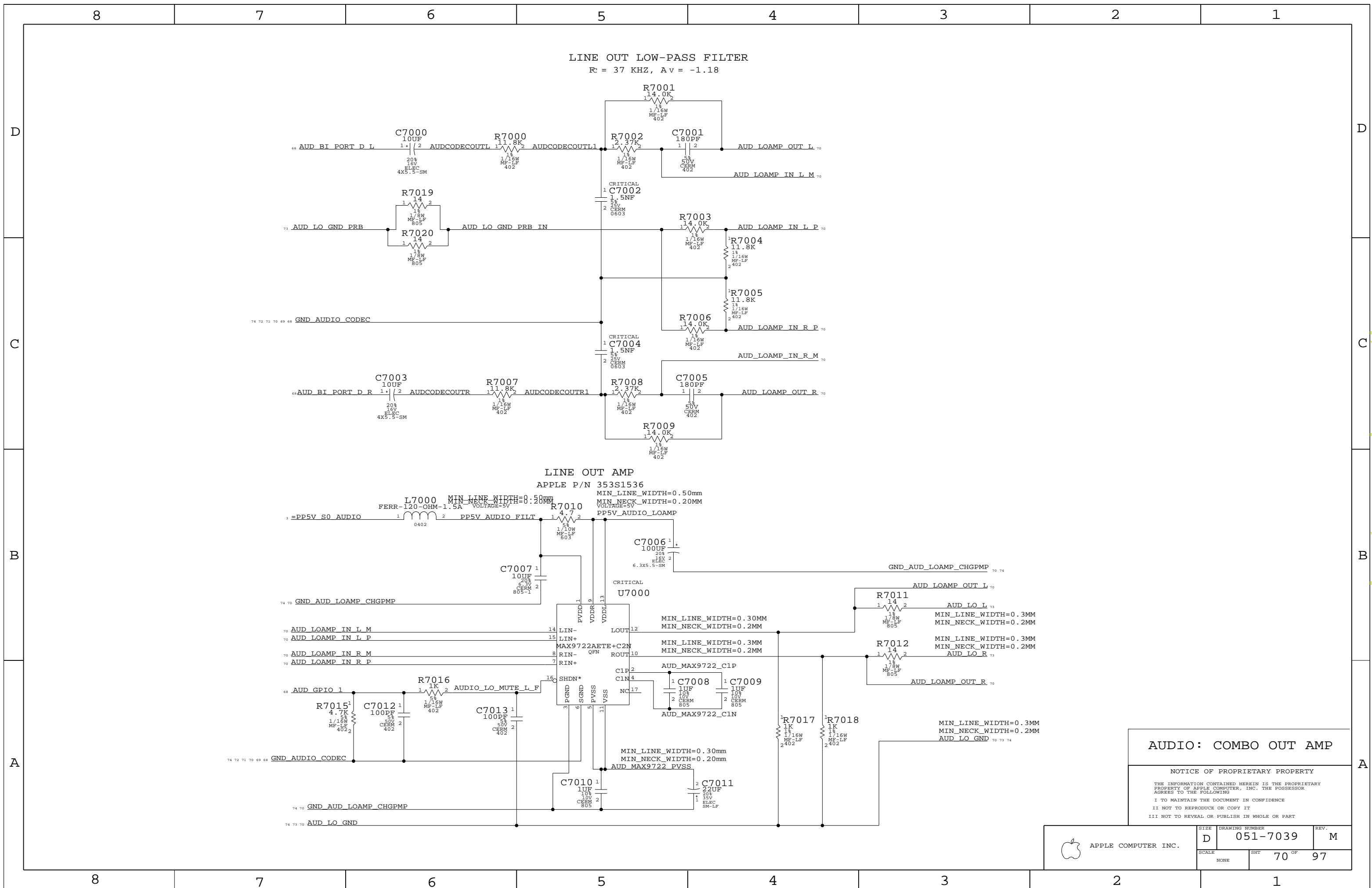
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7039	REV. M
	SCALE NONE	SHT 68 OF 97	



AUDIO: LINE INPUT AMP

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7039	M
SCALE	SHT	69 OF 97	
NONE			



LINE OUT LOW-PASS FILTER
 $F_c = 37 \text{ KHZ}, A_v = -1.18$

LINE OUT AMP
 APPLE P/N 353S1536

AUDIO: COMBO OUT AMP

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7039	M
SCALE	SHT	70 OF	97
NONE			

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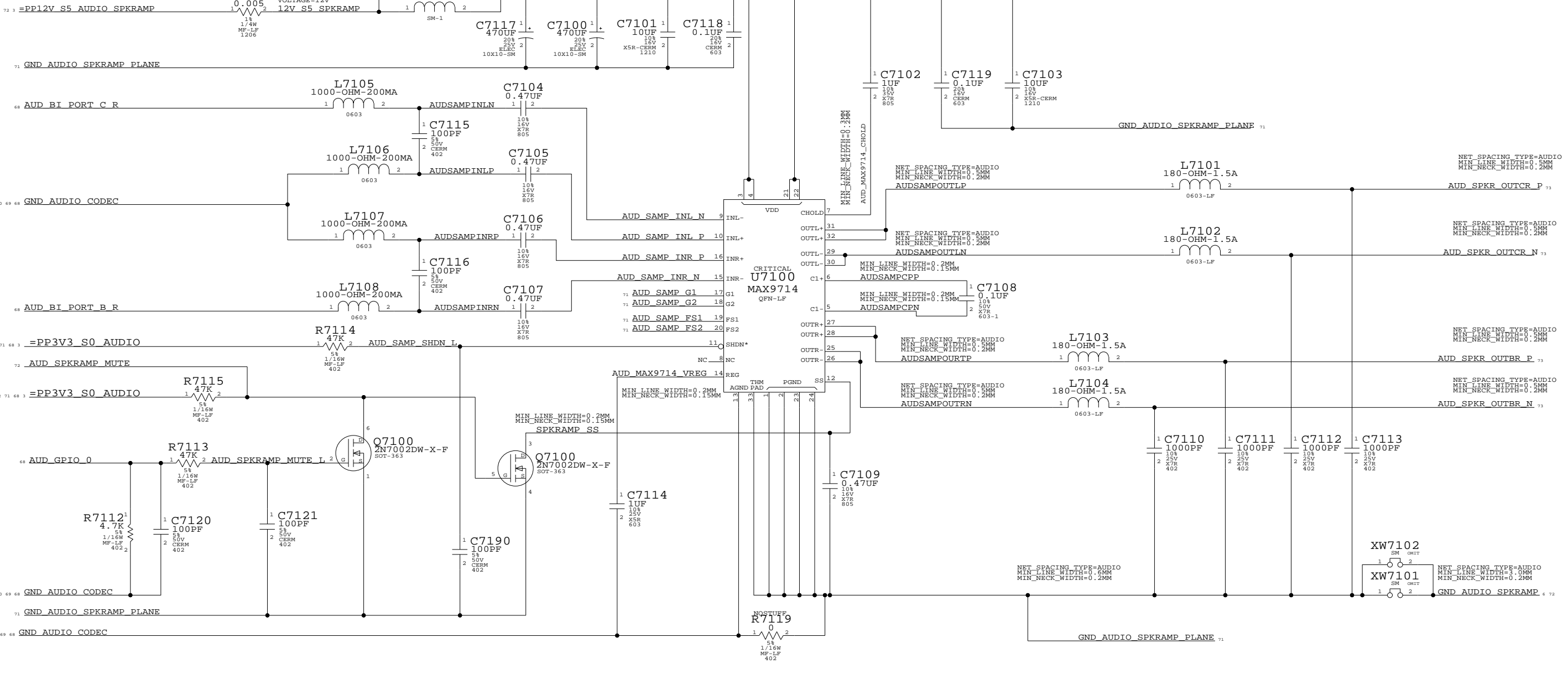
DRAWS NO POWER DURING S5
ONLY ON S5 RAIL TO AID ROUTING

SPEAKER AMP
APPLE P/N 353S1156

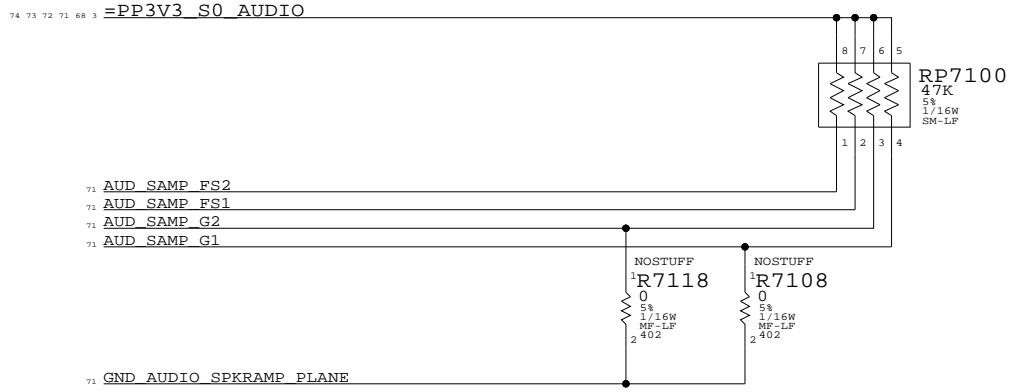
NET SPACING TYPE=AUDIO
MIN LINE WIDTH=3.0MM
MIN NECK WIDTH=0.2MM
VOLTAGE=12V

NET SPACING TYPE=AUDIO
MIN LINE WIDTH=3.0MM
MIN NECK WIDTH=0.2MM
VOLTAGE=12V

NET SPACING TYPE=AUDIO
MIN LINE WIDTH=1.5MM
MIN NECK WIDTH=0.2MM
VOLTAGE=12V



GAIN SETTINGS: +16DB
MODULATION SETTING: LOW EMI
GAIN AND SWITCHING FREQUENCY STUFF OPTIONS



AUDIO: SPEAKER AMP_1

SYNC_MASTER=AUDIO SYNC_DATE=08/04/2006

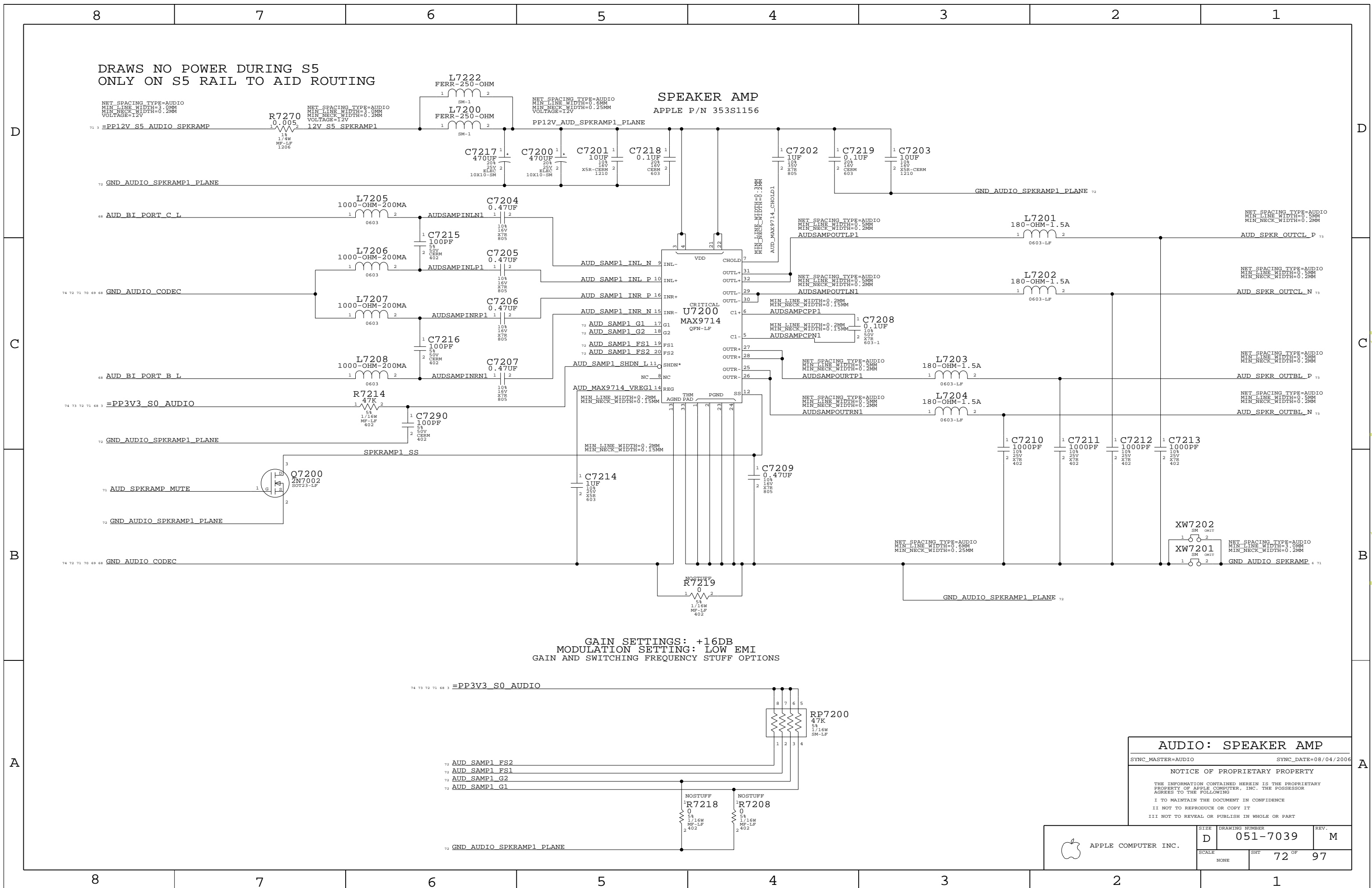
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7039	M
SCALE	SHT	71 OF	97
NONE			

DRWS NO POWER DURING S5
ONLY ON S5 RAIL TO AID ROUTING

SPEAKER AMP
APPLE P/N 353S1156

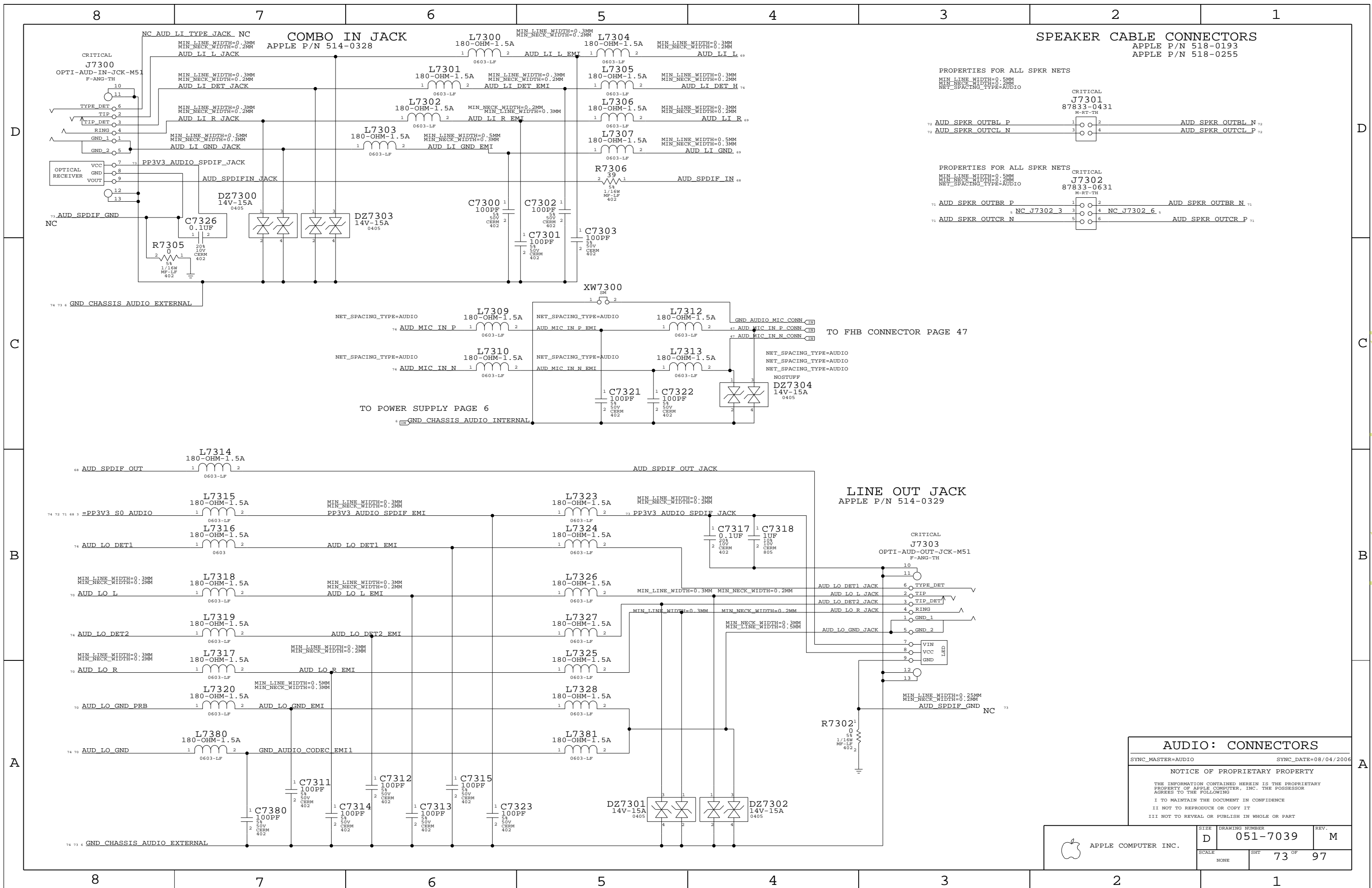


GAIN SETTINGS: +16DB
MODULATION SETTING: LOW EMI
GAIN AND SWITCHING FREQUENCY STUFF OPTIONS

AUDIO: SPEAKER AMP
SYNC_MASTER=AUDIO SYNC_DATE=08/04/2006
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7039	M
SCALE	SHT	72 OF 97	
NONE			

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AUDIO: CONNECTORS
 SYNC_MASTER=AUDIO SYNC_DATE=08/04/2006
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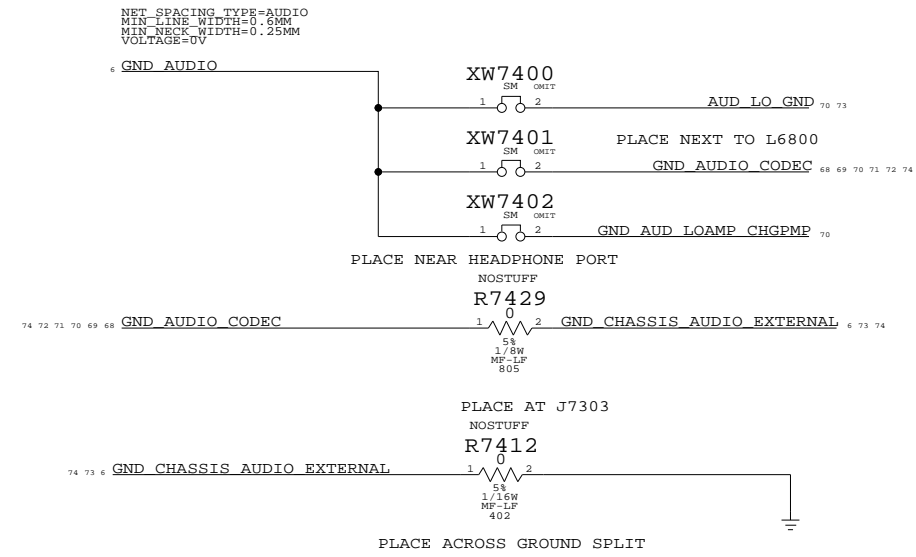
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7039	M
SCALE	SHT	73 OF	97
NONE			

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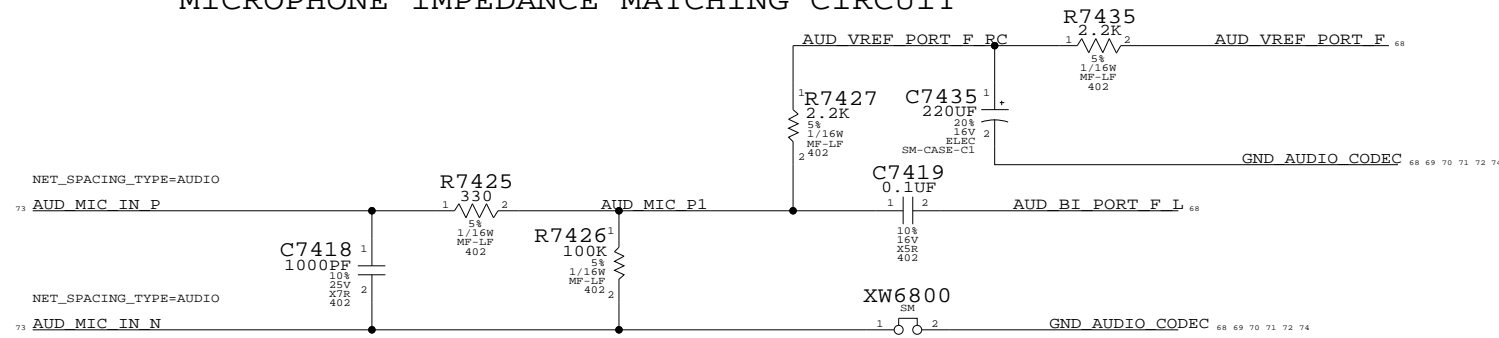
CODEC OUTPUT SIGNAL PATHS				
FUNCTION	VOLUME	DAC	PIN COMPLEX	MUTE CONTROL
LINE OUT	0X0C	0X02	0X14 (D)	GPIO 1
SPKR AMP	0X0D	0X03	0X18 (B)	GPIO 0
SPKR AMP1	0X0F	0X05	0X1A (C)	GPIO 0
SPDIFOUT		CONVERTER=0X06 PIN=0X1E		
		DETECT DELEGATE PIN 0X16H		

CODEC INPUT SIGNAL PATHS				
FUNCTION	ADC	MIXER	PORT	VREF
MIC INPUT	0X07	0X24	0X19 (F)	80%
LINE INPUT	0X08	0X23	0X15 (A)	50%
SPDIFIN	CONVERTER=0X0A		PIN=0X1F	

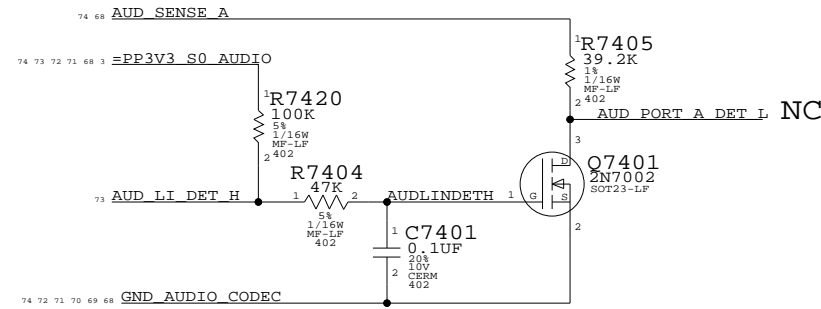
AUDIO GROUND RETURNS



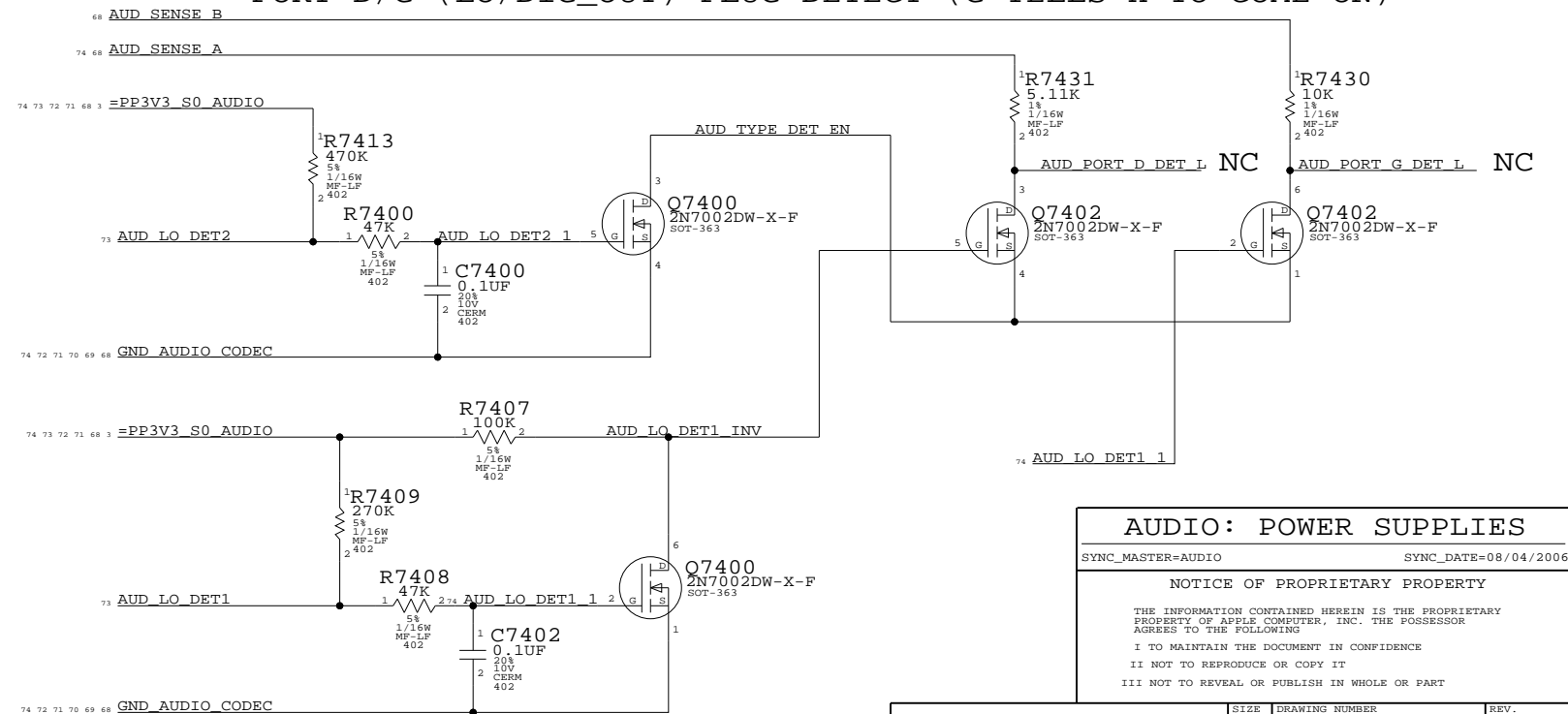
MICROPHONE IMPEDANCE MATCHING CIRCUIT



PORT A (LI) PLUG DETECT



PORT D/G (LO/DIG_OUT) PLUG DETECT (G TELLS H TO COME ON)



AUDIO: POWER SUPPLIES

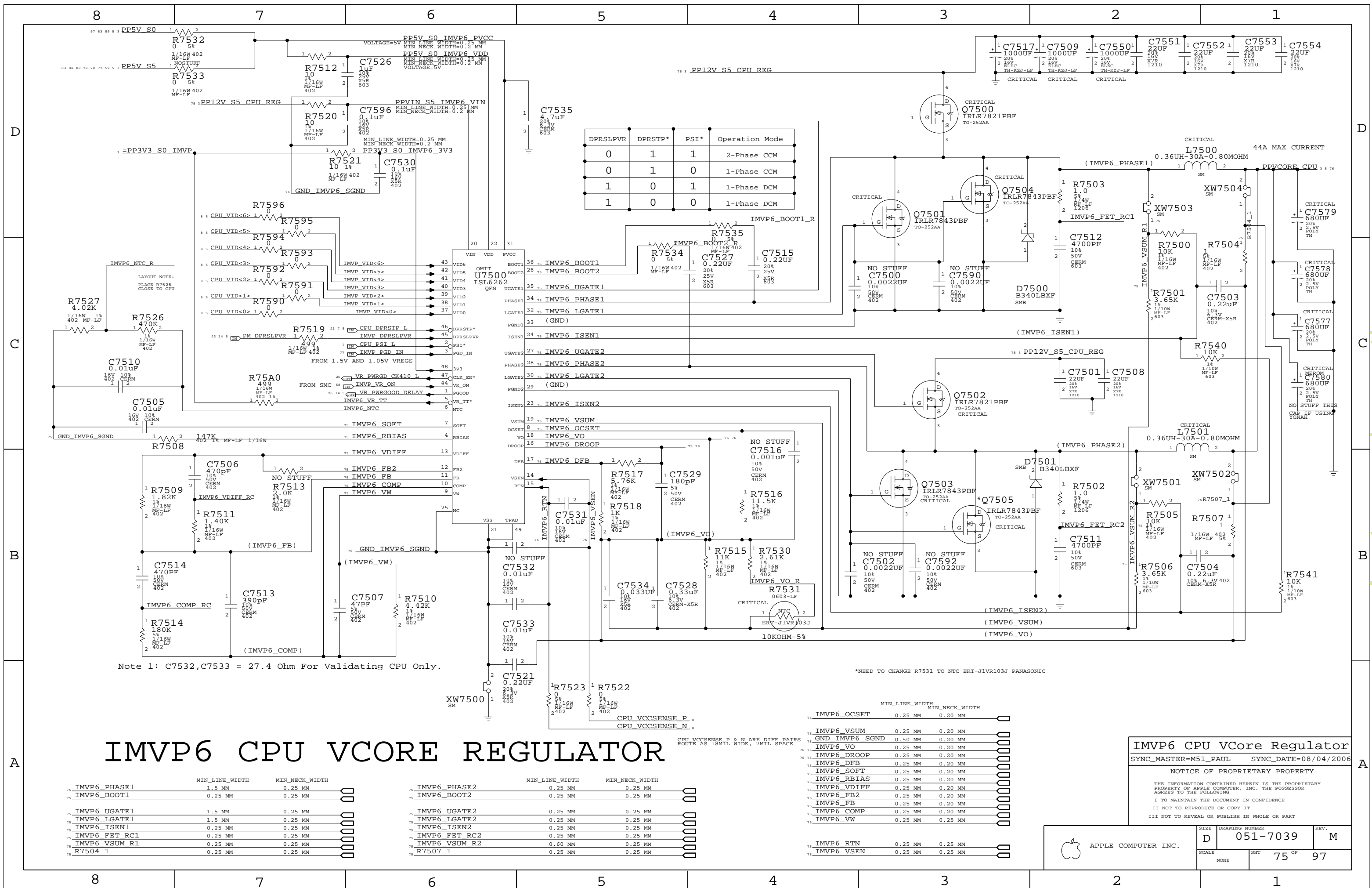
SYNC_MASTER=AUDIO SYNC_DATE=08/04/2006

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	D	051-7039	M
SCALE	SHT	74 OF 97	
NONE			



DPRSLPVR	DPRSTP*	PSI*	Operation Mode
0	1	1	2-Phase CCM
0	1	0	1-Phase CCM
1	0	1	1-Phase DCM
1	0	0	1-Phase DCM

IMVP6_BOOT1	IMVP6_BOOT2	IMVP6_UGATE1	IMVP6_UGATE2	IMVP6_PHASE1	IMVP6_PHASE2	IMVP6_LGATE1	IMVP6_LGATE2	IMVP6_ISEN1	IMVP6_ISEN2	IMVP6_VSUM	IMVP6_VSEN
NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF

Note 1: C7532,C7533 = 27.4 Ohm For Validating CPU Only.

*NEED TO CHANGE R7531 TO NTC ERT-J1VR103J PANASONIC

IMVP6 CPU VCore Regulator

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
75 IMVP6_PHASE1	1.5 MM	0.25 MM
75 IMVP6_BOOT1	0.25 MM	0.25 MM
75 IMVP6_UGATE1	1.5 MM	0.25 MM
75 IMVP6_LGATE1	1.5 MM	0.25 MM
75 IMVP6_ISEN1	0.25 MM	0.25 MM
75 IMVP6_FET_RC1	0.25 MM	0.25 MM
75 IMVP6_VSUM_R1	0.25 MM	0.25 MM
75 R7504_1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
75 IMVP6_PHASE2	0.25 MM	0.25 MM
75 IMVP6_BOOT2	0.25 MM	0.25 MM
75 IMVP6_UGATE2	0.25 MM	0.25 MM
75 IMVP6_LGATE2	0.25 MM	0.25 MM
75 IMVP6_ISEN2	0.25 MM	0.25 MM
75 IMVP6_FET_RC2	0.25 MM	0.25 MM
75 IMVP6_VSUM_R2	0.60 MM	0.25 MM
75 R7507_1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
75 IMVP6_OCSET	0.25 MM	0.20 MM
75 IMVP6_VSUM	0.25 MM	0.20 MM
75 GND_IMVP6_SGND	0.50 MM	0.20 MM
75 IMVP6_VO	0.25 MM	0.20 MM
75 IMVP6_DROOP	0.25 MM	0.20 MM
75 IMVP6_DFB	0.25 MM	0.20 MM
75 IMVP6_SOFT	0.25 MM	0.20 MM
75 IMVP6_VDIFF	0.25 MM	0.20 MM
75 IMVP6_FB2	0.25 MM	0.20 MM
75 IMVP6_FB	0.25 MM	0.20 MM
75 IMVP6_COMP	0.25 MM	0.20 MM
75 IMVP6_VW	0.25 MM	0.25 MM
75 IMVP6_RTIN	0.25 MM	0.25 MM
75 IMVP6_VSEN	0.25 MM	0.25 MM

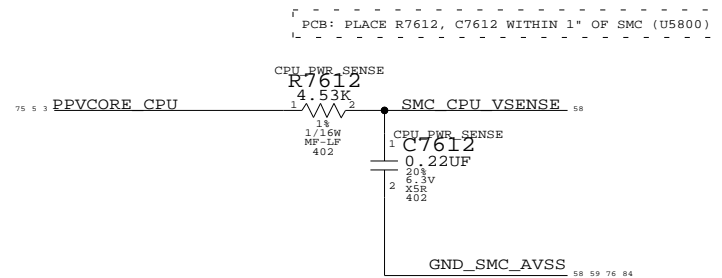
IMVP6 CPU VCore Regulator
 SYNC_MASTER=M51_PAUL SYNC_DATE=08/04/2006

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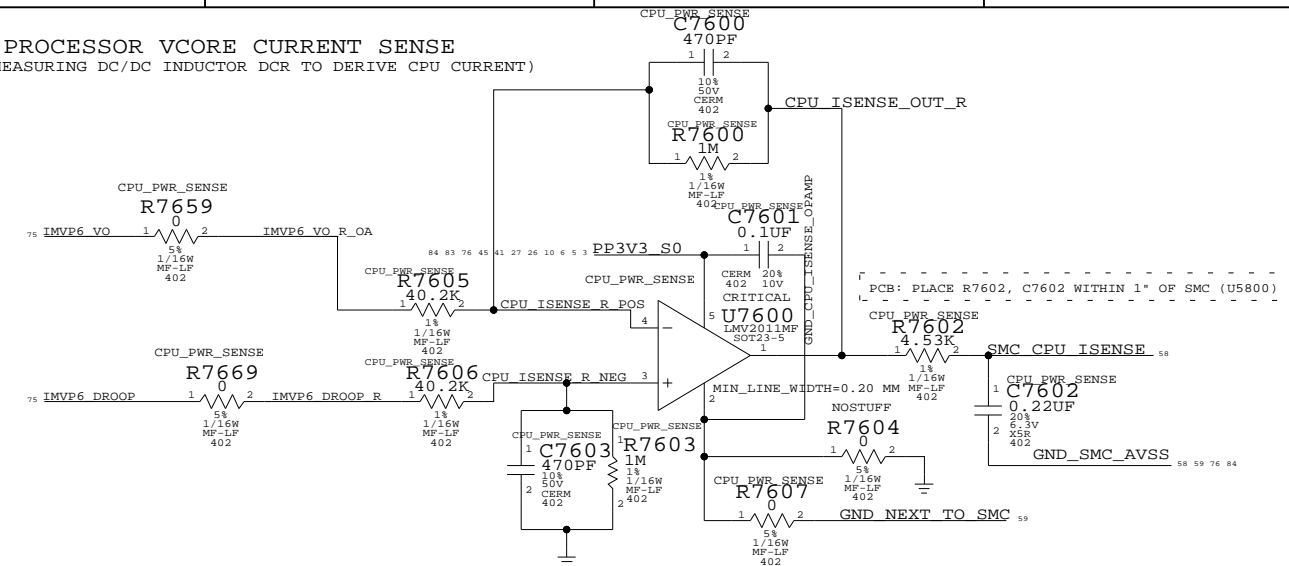
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7039	M
SCALE	SHEET	75 OF 97	
NONE			

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PROCESSOR VCORE SENSE

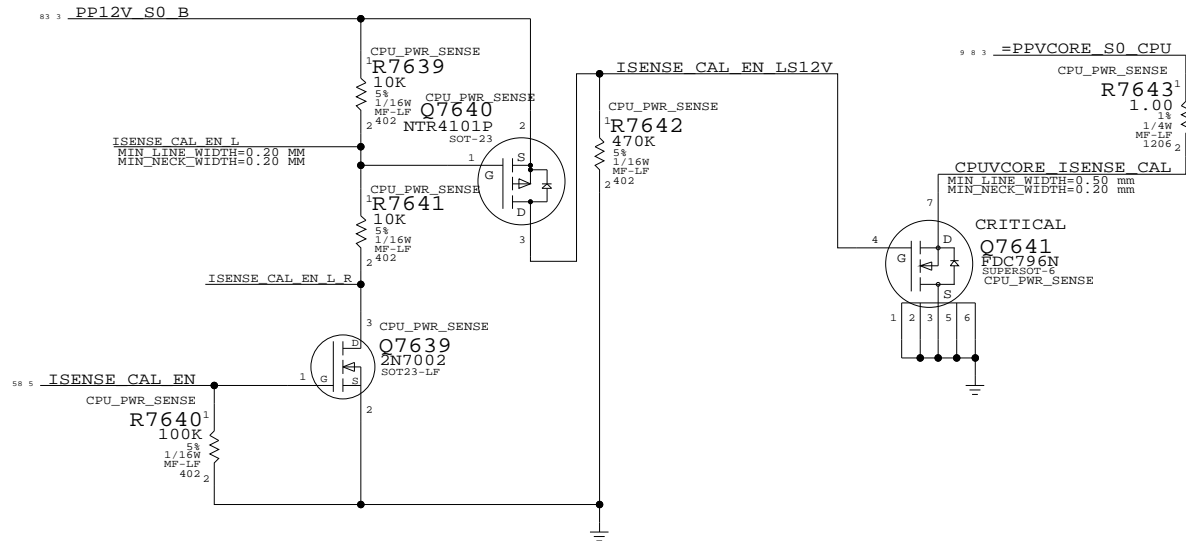


PROCESSOR VCORE CURRENT SENSE
(MEASURING DC/DC INDUCTOR DCR TO DERIVE CPU CURRENT)

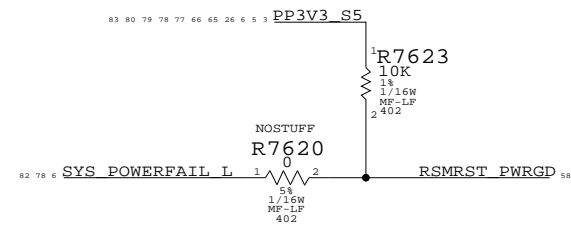


CPU CURRENT SENSE CALIBRATION CIRCUIT

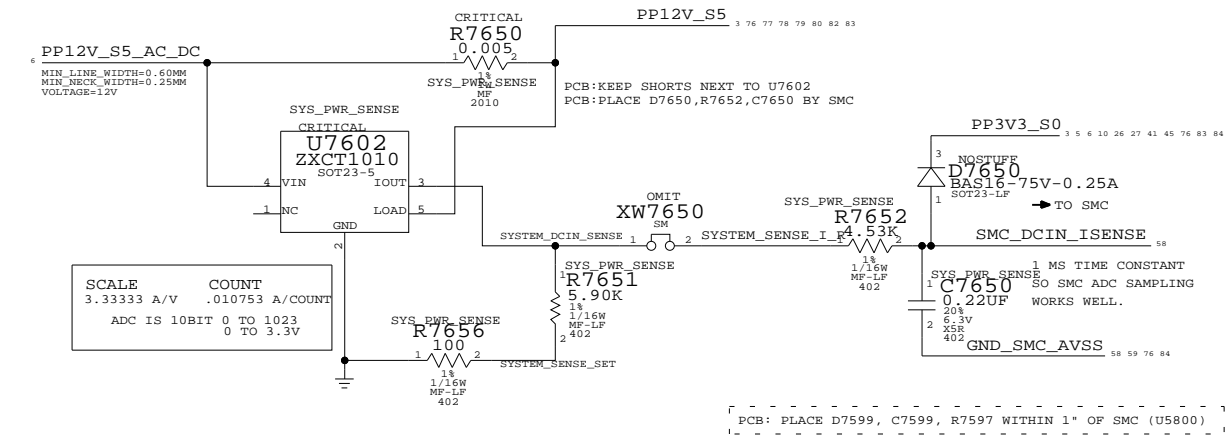
Switches in fixed load on power supplies to calibrate current sense circuits



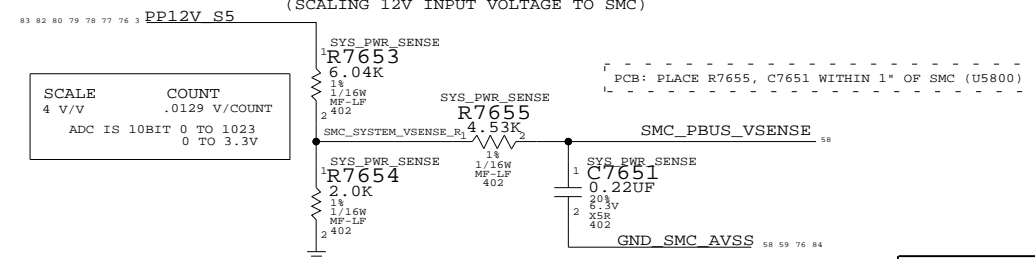
SMC PWRGD PULLUP



SYSTEM CURRENT SENSE



SYSTEM VOLTAGE SENSE
(SCALING 12V INPUT VOLTAGE TO SMC)



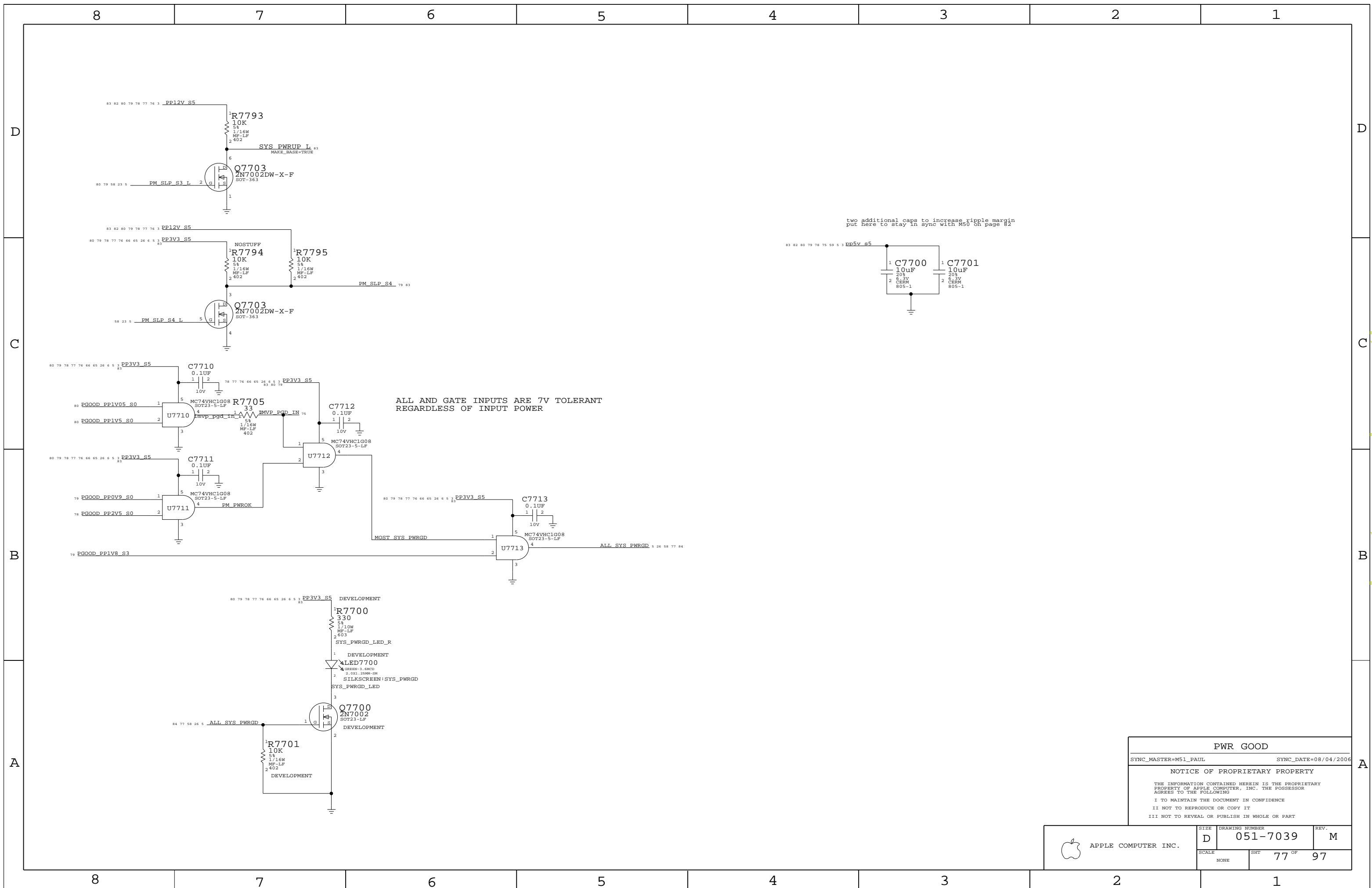
CPU & SYSTEM SENSE

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

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	D	051-7039	M
SCALE	SHT	76 OF	97
NONE			



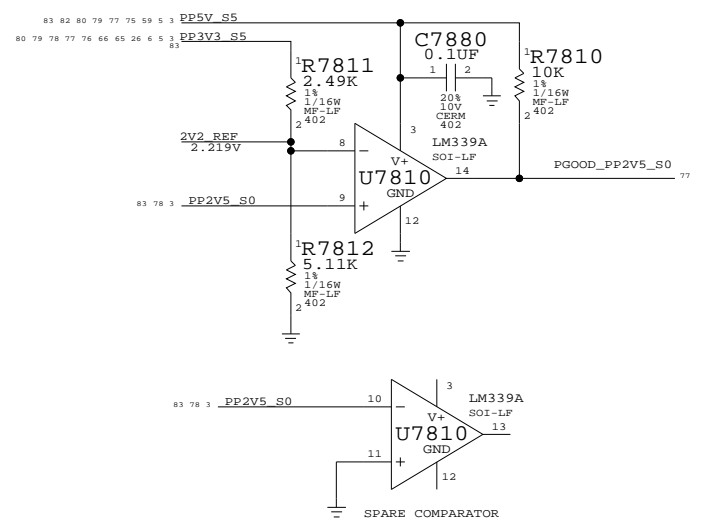
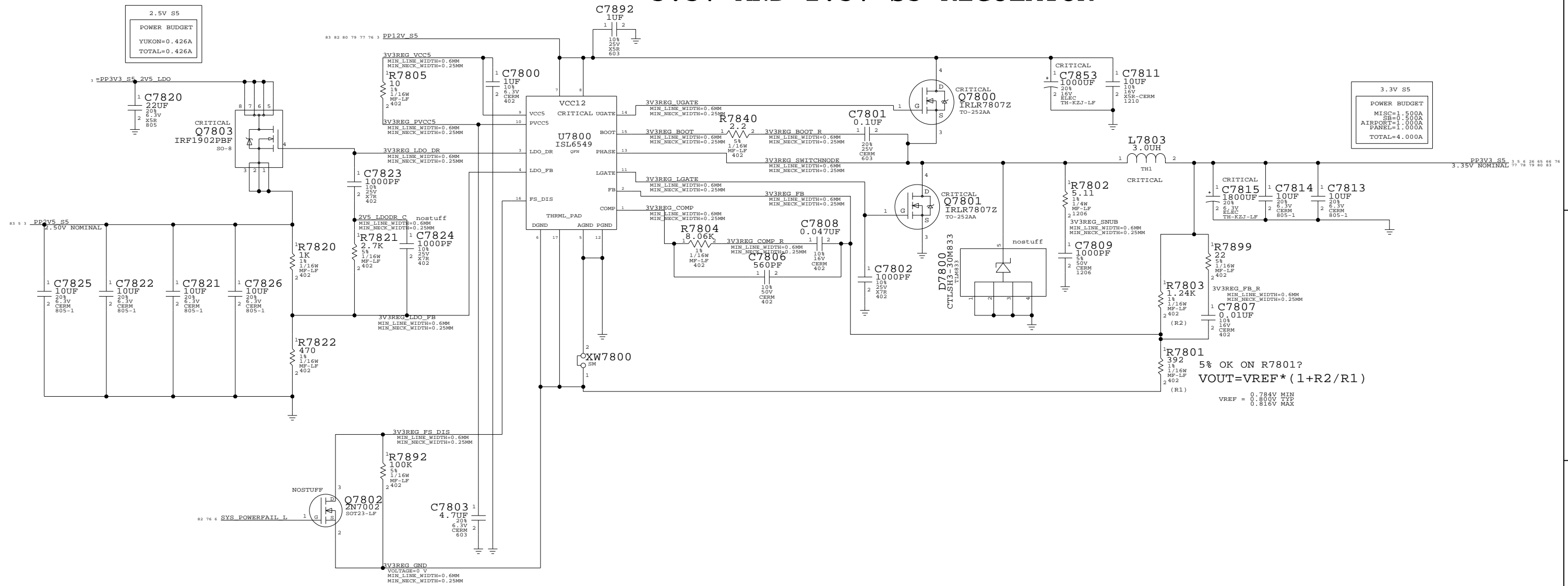
ALL AND GATE INPUTS ARE 7V TOLERANT
REGARDLESS OF INPUT POWER

two additional caps to increase ripple margin
put here to stay in sync with M50 on page 82

PWR GOOD	
SYNC_MASTER=M51_PAUL	SYNC_DATE=08/04/2006
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 APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7039	REV. M
	SCALE NONE	SHT 77 OF	97

3.3V AND 2.5V S5 REGULATOR



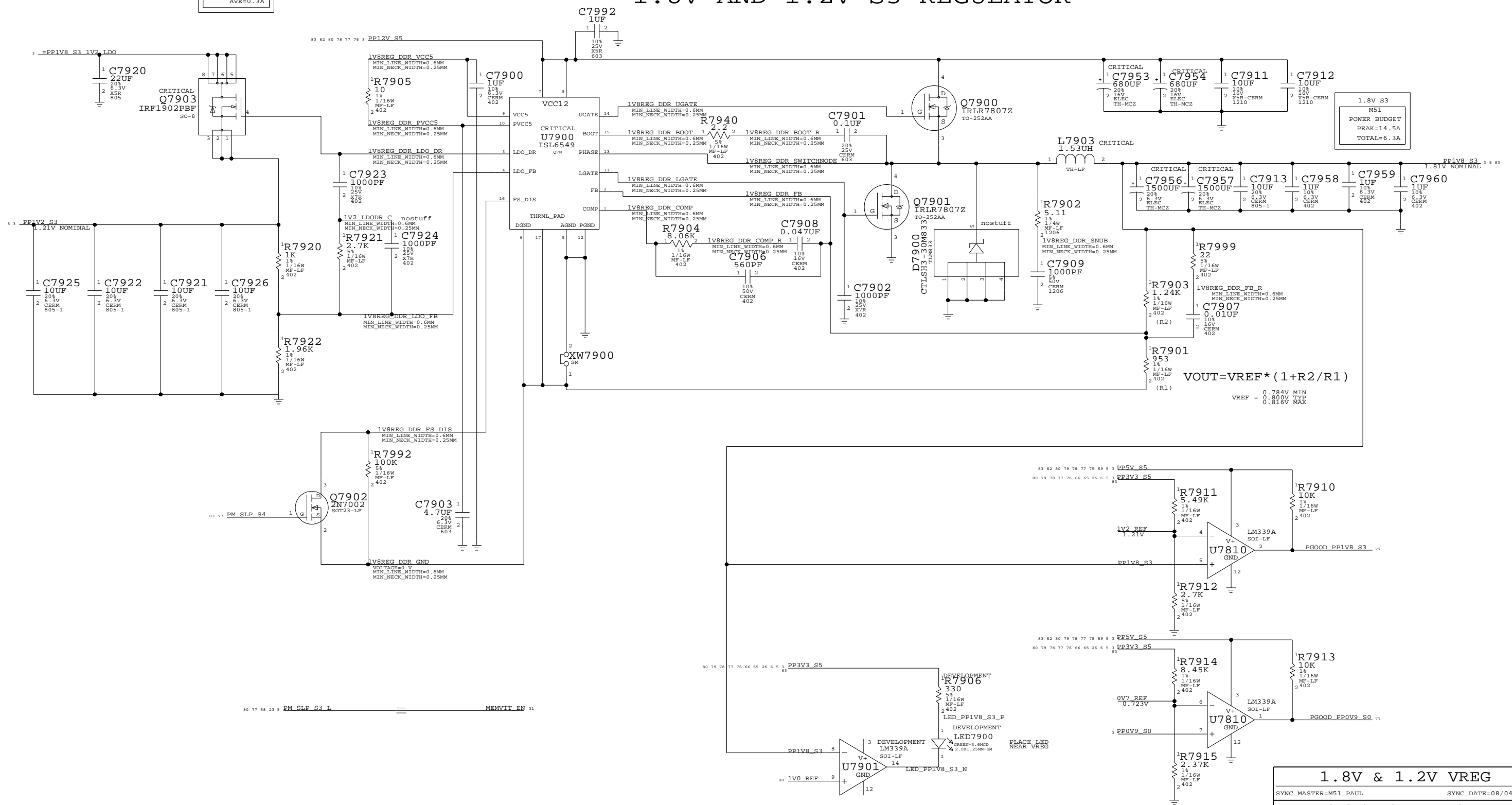
3V DC/DC 2.5V
 SYNC_MASTER=M51_PAUL SYNC_DATE=08/04/2006
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	D	051-7039	M
SCALE	SHT	78 OF 97	
NONE			

1.8V AND 1.2V S3 REGULATOR

1.2V S3
POWER BUDGET
PEAK=0.4A
AVE=0.3A

1.8V S3
M51
POWER BUDGET
PEAK=14.5A
TOTAL=6.3A



$$V_{OUT} = V_{REF} * (1 + R_2/R_1)$$

$V_{REF} = 0.784V \text{ MIN}$
 $V_{REF} = 0.810V \text{ TYP}$
 $V_{REF} = 0.816V \text{ MAX}$

1.8V & 1.2V VREG

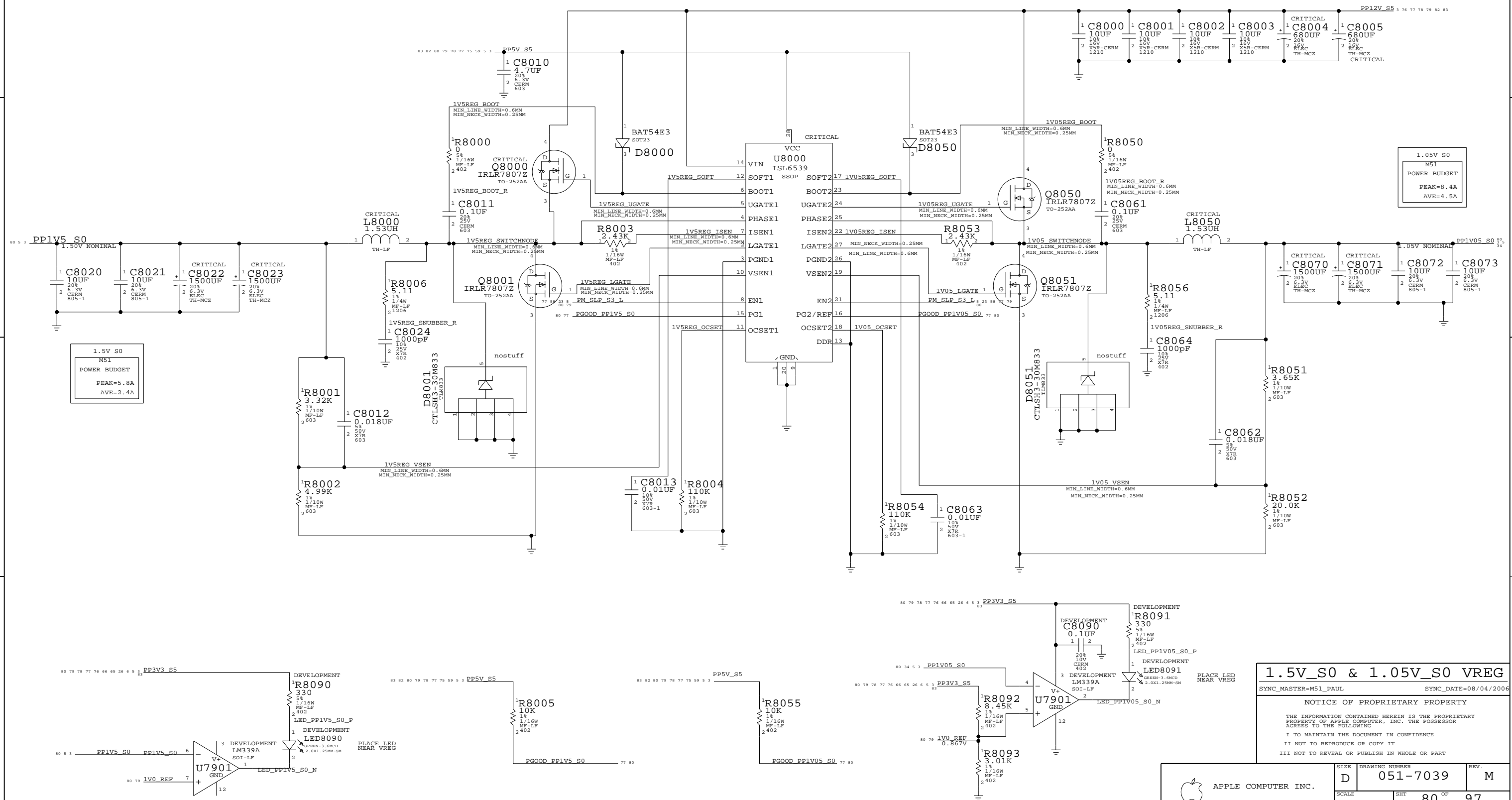
SYNC_MASTER=M51_PAUL SYNC_DATE=08/04/2006

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	D	051-7039	M
SCALE	SHT	79 OF 97	
NONE			

1.5V S0 AND 1.05V S0 RAILS



1.5V S0
M51
POWER BUDGET
PEAK=5.8A
AVE=2.4A

1.05V S0
M51
POWER BUDGET
PEAK=8.4A
AVE=4.5A

1.5V_S0 & 1.05V_S0 VREG

SYNC_MASTER=M51_PAUL SYNC_DATE=08/04/2006

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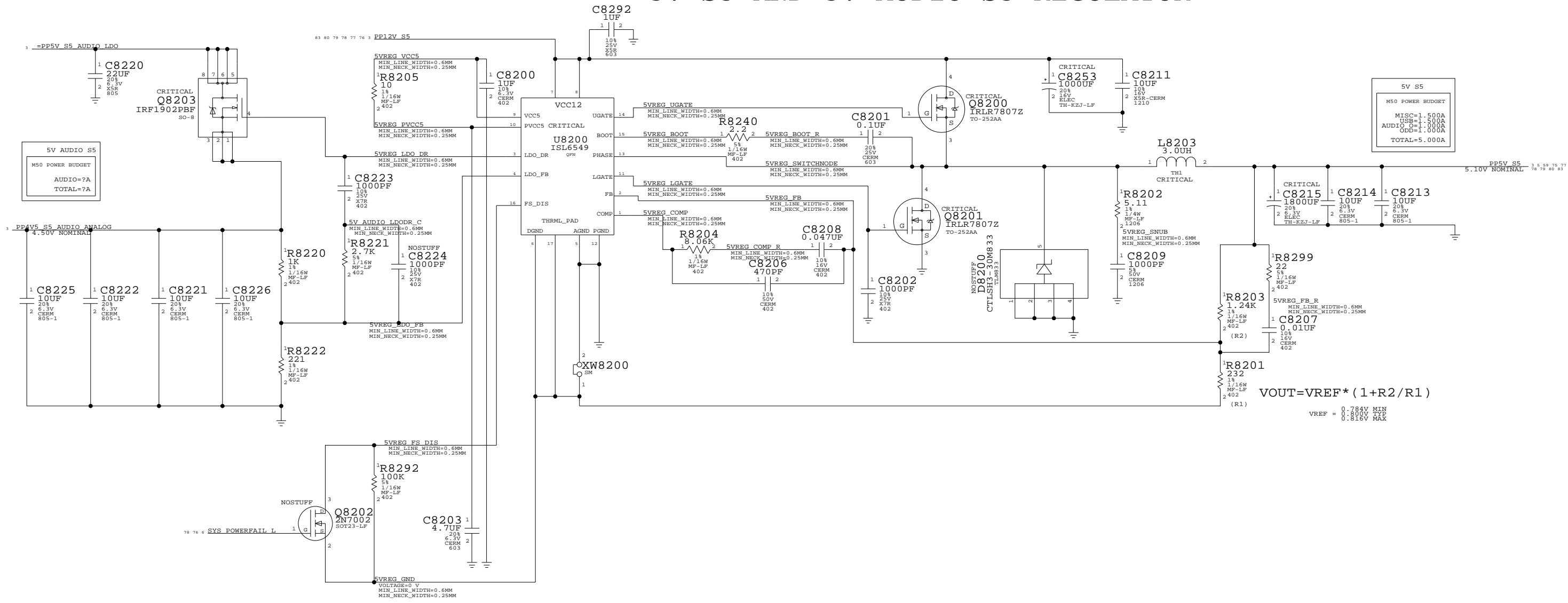
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7039	M
SCALE	SHT	80 OF	97
NONE			

5V S5 AND 5V AUDIO S5 REGULATOR



5V AUDIO S5
M50 POWER BUDGET
AUDIO=7A
TOTAL=7A

5V S5
M50 POWER BUDGET
MISC=1.500A
USB=1.500A
AUDIO_ODD=1.000A
TOTAL=5.000A

$$V_{OUT} = V_{REF} * (1 + R2/R1)$$

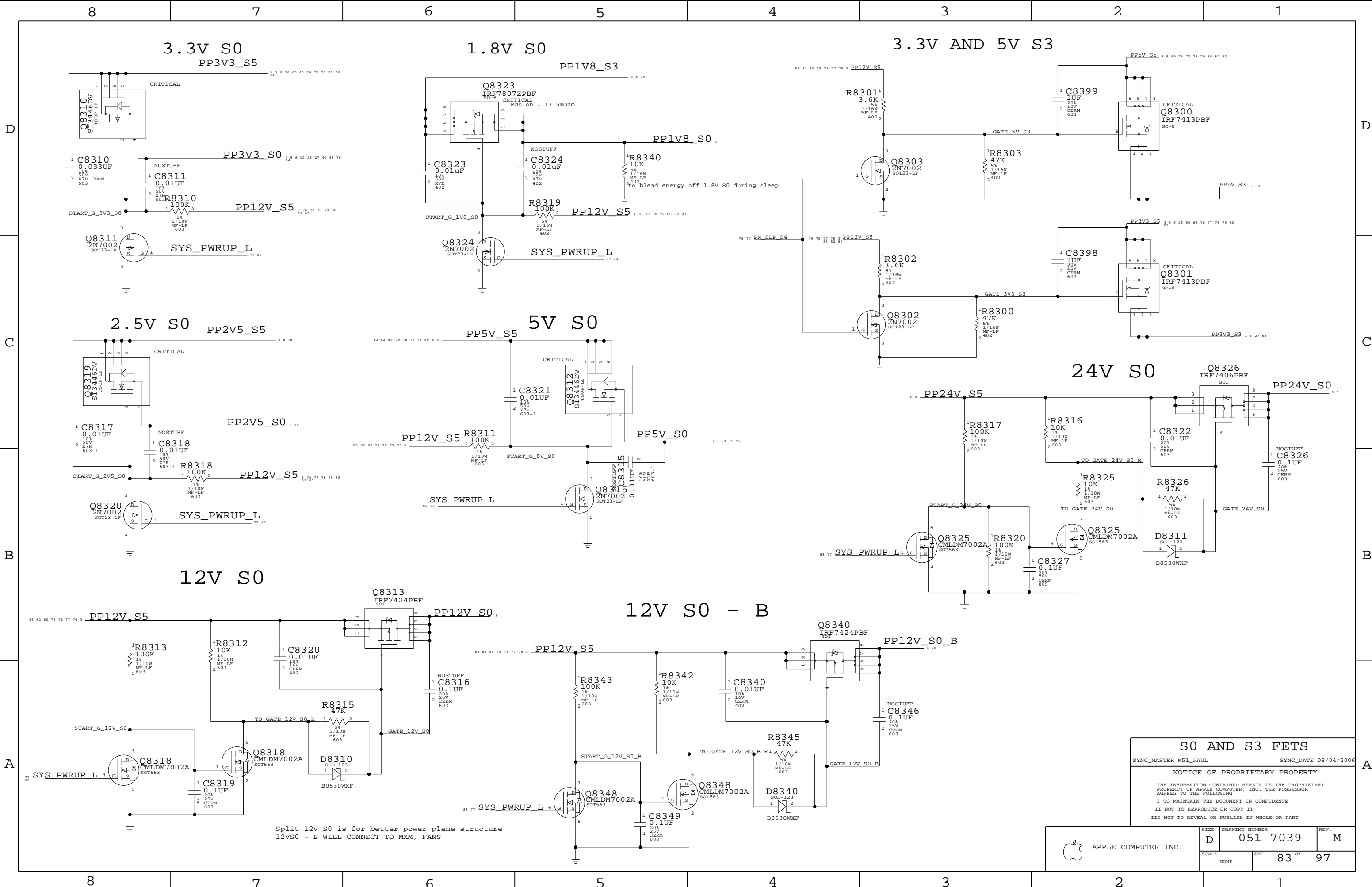
VREF = 0.784V MIN
0.800V TYP
0.816V MAX

POWER SUPPLY 3.3V/5V MAIN SWITCH

5V DC/DC	
SYNC_MASTER=M51_PAUL	SYNC_DATE=08/04/2006
NOTICE OF PROPRIETARY PROPERTY	
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NONE			

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Split 12V S0 is for better power plane structure
12VS0 - B WILL CONNECT TO MXM, FANS

S0 AND S3 FETS
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Page Notes

Power aliases required by this page:

- =PP12V_S0_MXM
- =PP5V_S0_MXM
- =PP1V8_S0_MXM

Signal aliases required by this page:
(NONE)

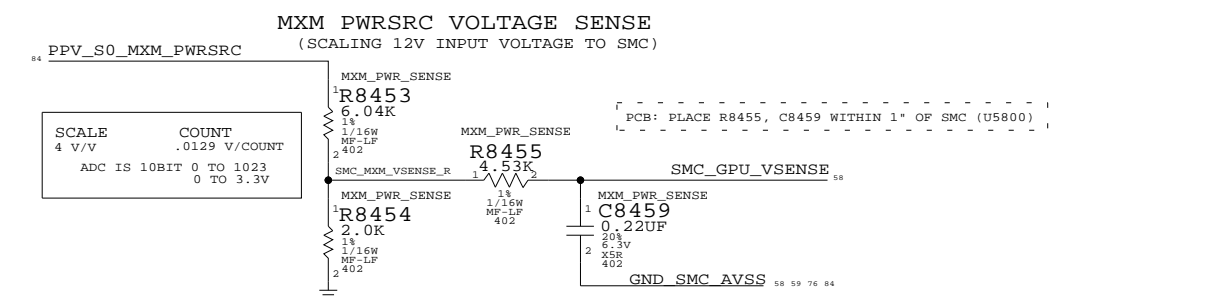
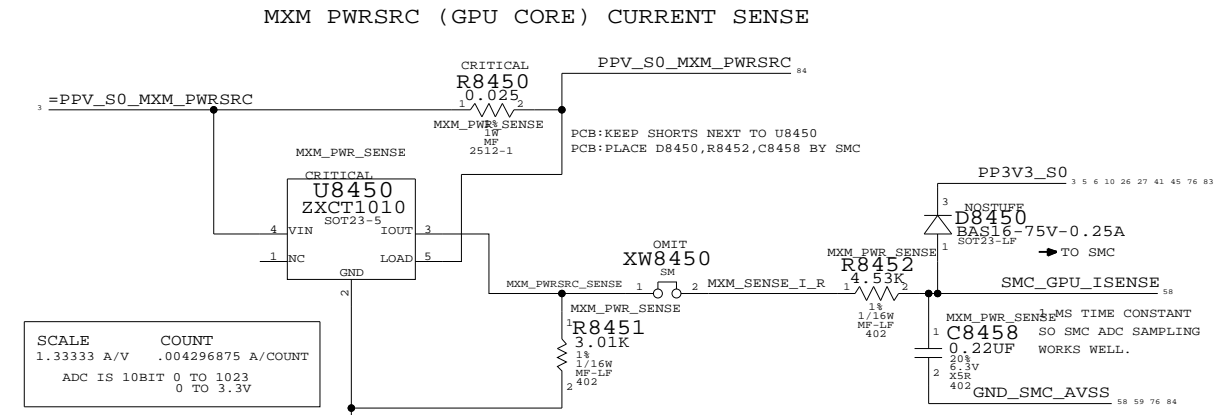
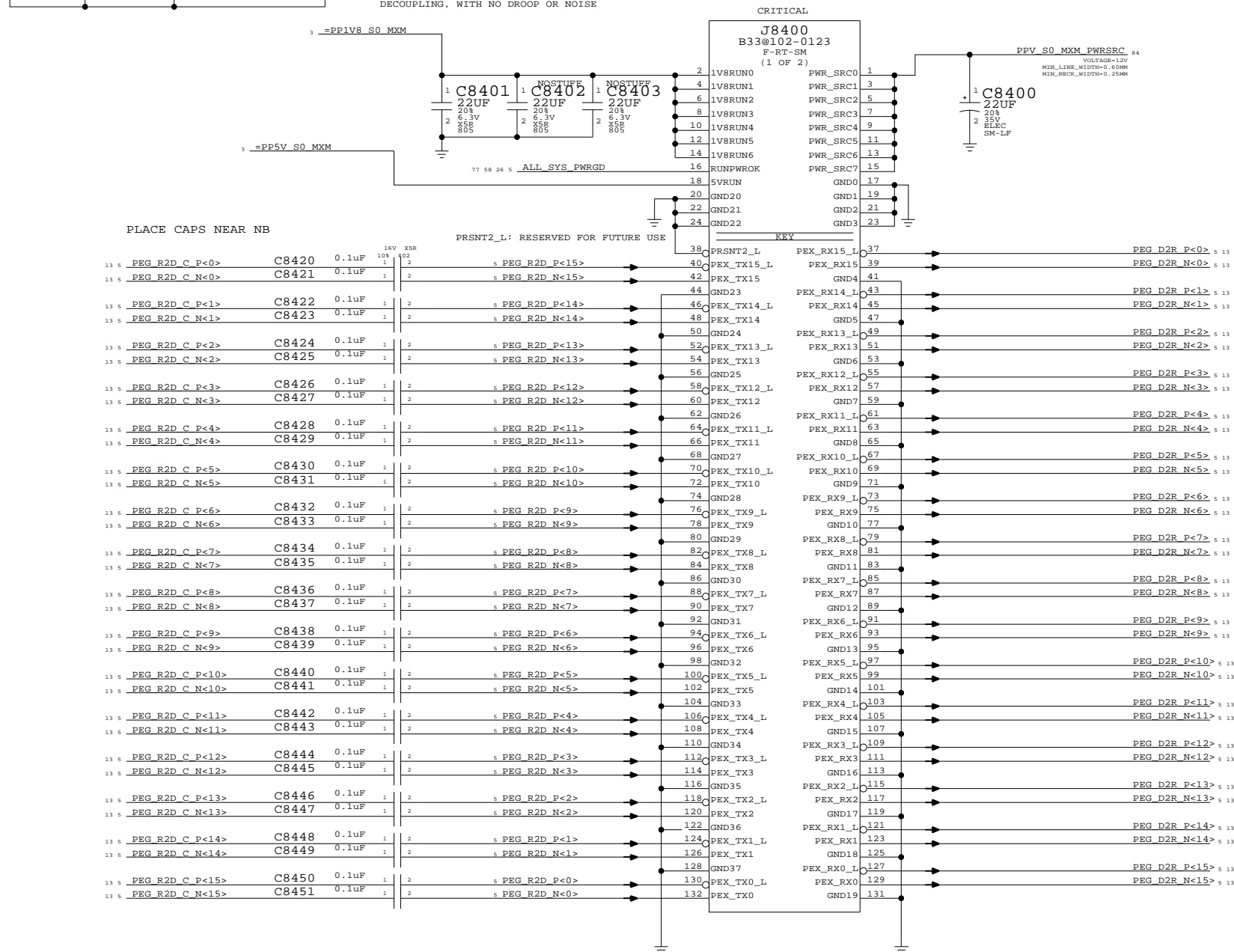
BOM options provided by this page:
(NONE)

Note: PCI-E Lanes are reversed to untangle routes
Need to stuff config strap using BOM option NBCFG_PEG_REVERSE
Polarity is also inverted (Tx+ goes to Rx-) to untangle routes

MXM SPEC POWER REQUIREMENTS
(NOT NECESSARILY THE SAME FOR EVERY MODULE)

VOLTAGE	CURRENT	POWER
3V3	1.5 A	4.95 W
5V	0.5 A	2.5 W
2V5	0.5 A	1.25 W
1V8	3.5 A	6.3 W
PWR (12V)	UP TO 4 A	PLATFORM DEPENDENT

M51: FIX ON CARD ALLOWS US TO NOT STUFF MOST OF THE 1.8V DECOUPLING, WITH NO DROOP OR NOISE



MXM PCI-E & PWR
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	D	051-7039	M
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NONE			

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Page Notes

Power aliases required by this page:
 - =PP3V3_S0_MXM
 - =PP2V5_S0_MXM

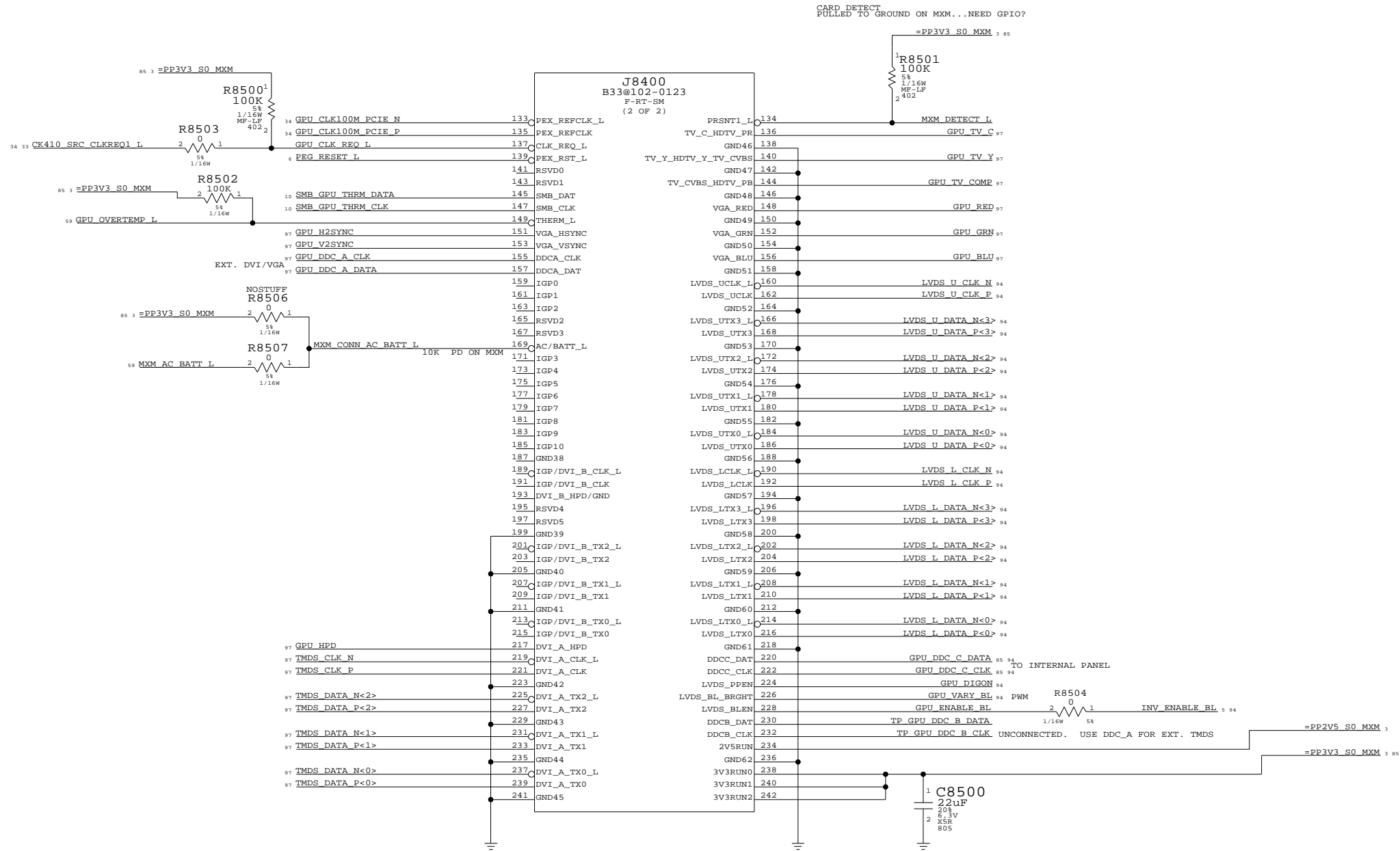
Signal aliases required by this page:
 - =SMB_GPU_THRM_DATA
 - =SMB_GPU_THRM_CLK

BOM options provided by this page:
 (NONE)

MXM SPEC POWER REQUIREMENTS

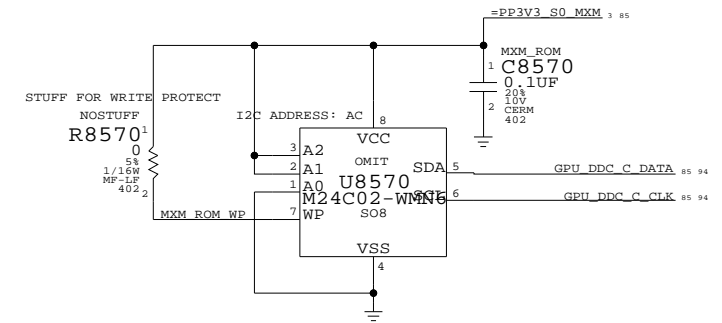
(NOT NECESSARILY THE SAME FOR EVERY MODULE)

VOLTAGE	CURRENT	POWER
3V3	1.5 A	4.95 W
5V	0.5 A	2.5 W
2V5	0.5 A	1.25 W
1V8	3.5 A	6.3 W
PWR (12V)	UP TO 4 A	PLATFORM DEPENDENT



MXM SYSTEM INFORMATION ROM

PLACE CLOSE TO J8400



MXM I/O	
SYNC_MASTER=M51_DAVE	SYNC_DATE=(MASTER)
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NONE			

Page Notes

Power aliases required by this page:
 - =PP12V_LCD
 - =PP24V_INVERTER
 - =PP3V3_S0_VIDEO

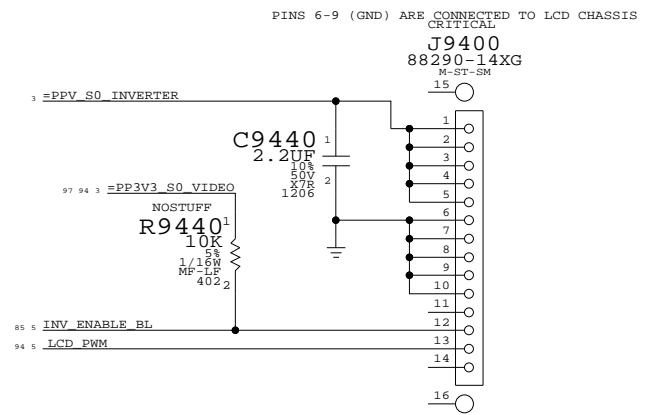
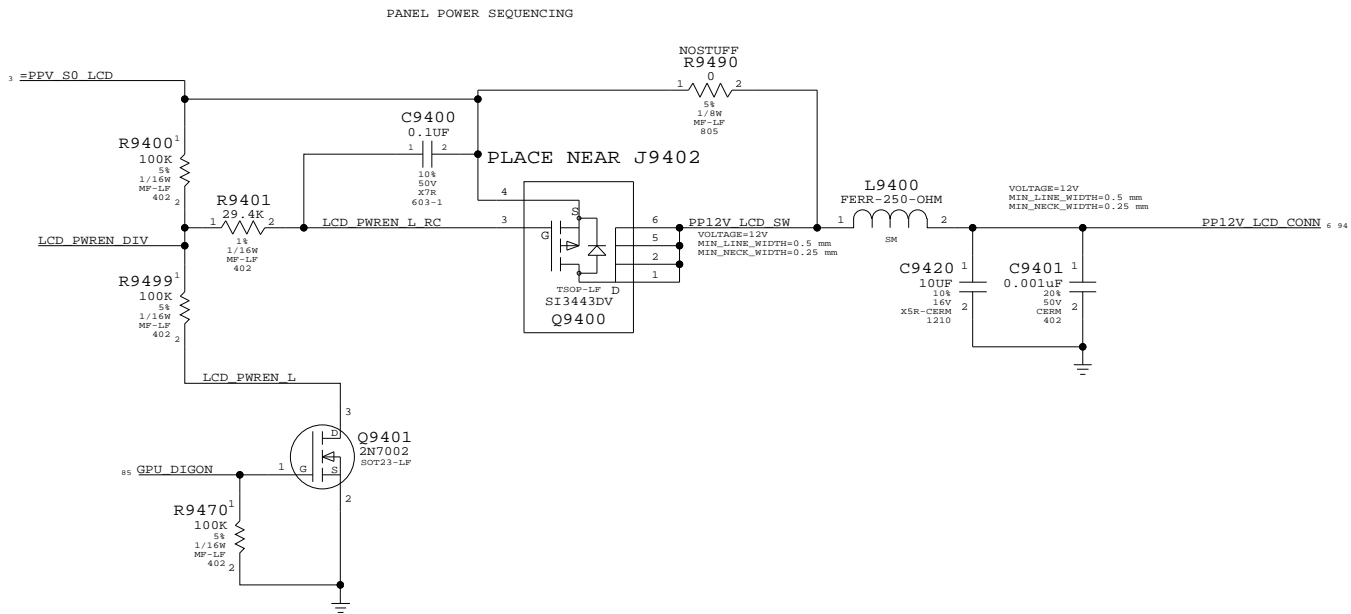
Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

97 94 3 =PP3V3_S0_VIDEO =PP3V3_DDC_LCD 94

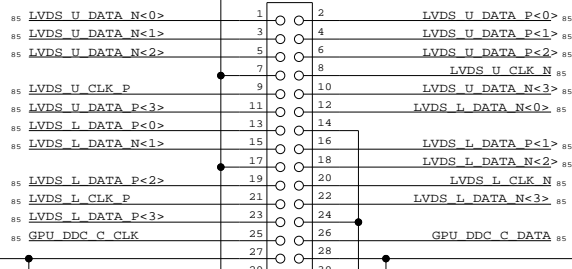
LCD (LVDS) INTERFACE

INVERTER INTERFACE



CRITICAL
SDF9400
STDOFF-3MMOD4.6MMH-1.35-TH

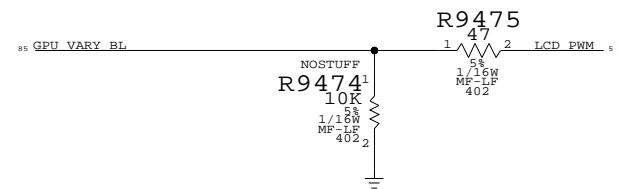
CRITICAL
J9402
53307-3072
F-ST-SM



Panel has 4.7K DDC pull-ups
 MXM also has 2.2K pull-ups

C9410
0.001uF
20V
50V
CERM
402

CRITICAL
SDF9401
STDOFF-3MMOD4.6MMH-1.35-TH



Internal Display Conns

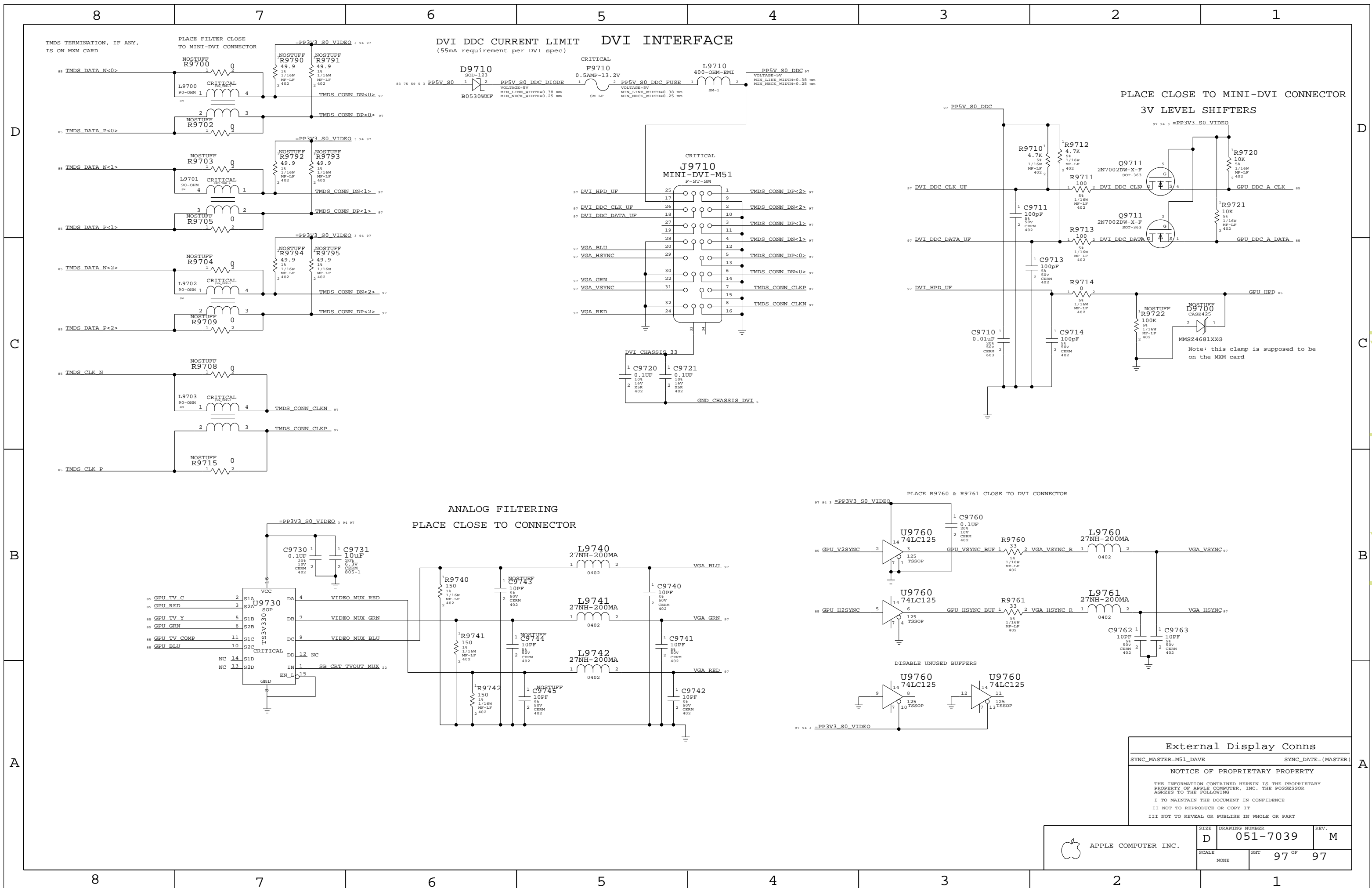
SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

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NONE			



External Display Conns
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	SCALE NONE	SHEET 97 OF 97	

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